TOSHIBA

NTDPJTV03

Technical Training Manual

"Customer Satisfaction Through Knowledge"

SERVICING THE TOSHIBA WIDE SCREEN PROJECTION TV TW56D90

TOSHIBA AMERICA CONSUMER PRODUCTS, INC.

"In Touch with Tomorrow"

FOREWORD

The material presented in this manual is provided for the technical training of TACP employees and qualified service personnel only.

The specific circuit reference designations, pin numbers, etc., are taken from the TW56D90 Service Manual, File Number 050-737. The diagrams in this manual are simplified for training and should be used as a guide only when servicing the TW56D90. Refer to the applicable service data for detailed adjustment and servicing procedures.

NOTE: ***This text contains only the items modified from those of the N2DB chassis.*** Accordingly, for those items not given here, refer to the Service Training Manual for the N2DB chassis (File no. NTDCTV04).

NTDPJTV03

SERVICING TOSHIBA'S TW56D90 WIDESCREEN PROJECTION TELEVISION

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SECTION I
INTRODUCTION

1. FEATURE

The TW56D90 is Toshiba's first PJ-TV with a wide screen aspect ratio of 16:9 to be introduced into North U.S.A. markets.

In order to display an image in the wide screen format, a WA (Wide Aspect) circuit is employed.

Moreover, a 3-dimensional Y/C separation circuit and a Dolby Pro Logic circuit are contained, complementing the features of this high end PJTV.

An important aspect of the TW56D90 is the use of the N2DB chassis. This chassis introduces a new bus system, developed by the PHILIPS company, called the I^2C (or IIC) bus. IIC stands for Inter-Integrated Circuit control. This bus coordinates the transfer of data and control between ICs inside the TV. It is a bi-directional serial bus consisting of two lines, named SDA (Serial DATA), and SCL (Serial CLOCK). This bus control system is made possible through the use of digital-to-analog converters built into the ICs, allowing them to be addressed and controlled by strings of digital instructions.

2. MERITS OF THE BUS SYSTEM

2-1. Improved Serviceability

Most of the adjustments previously made by resetting variable resistors and/or capacitors can be made on the new chassis by operating the remote control and seeing the results on the TV screen. This allows adjustments to be made without removing the back cover, thus improving servicing speed and efficiency.

2-2. Reduction of Parts Count

The use of digital-to-analog converters built into the ICs, allowing them to be controlled by software, has eliminated or reduced the requirement for many discrete parts such as potentiometers and trimmers, etc.

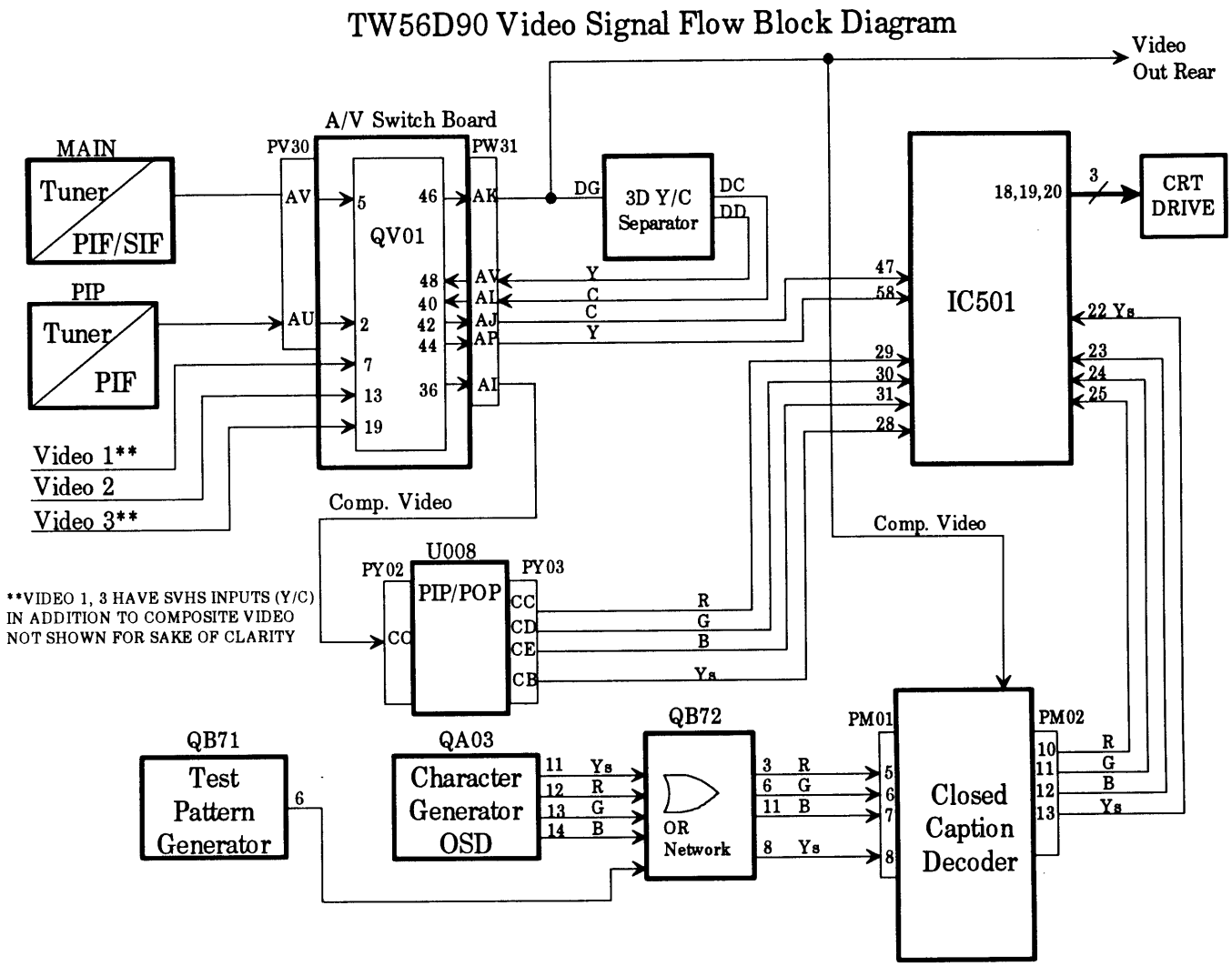
2-3. Quality Control

Centralized control of adjustment data makes it easier to understand, analyze, and review such data, thus improving the overall quality of the product.

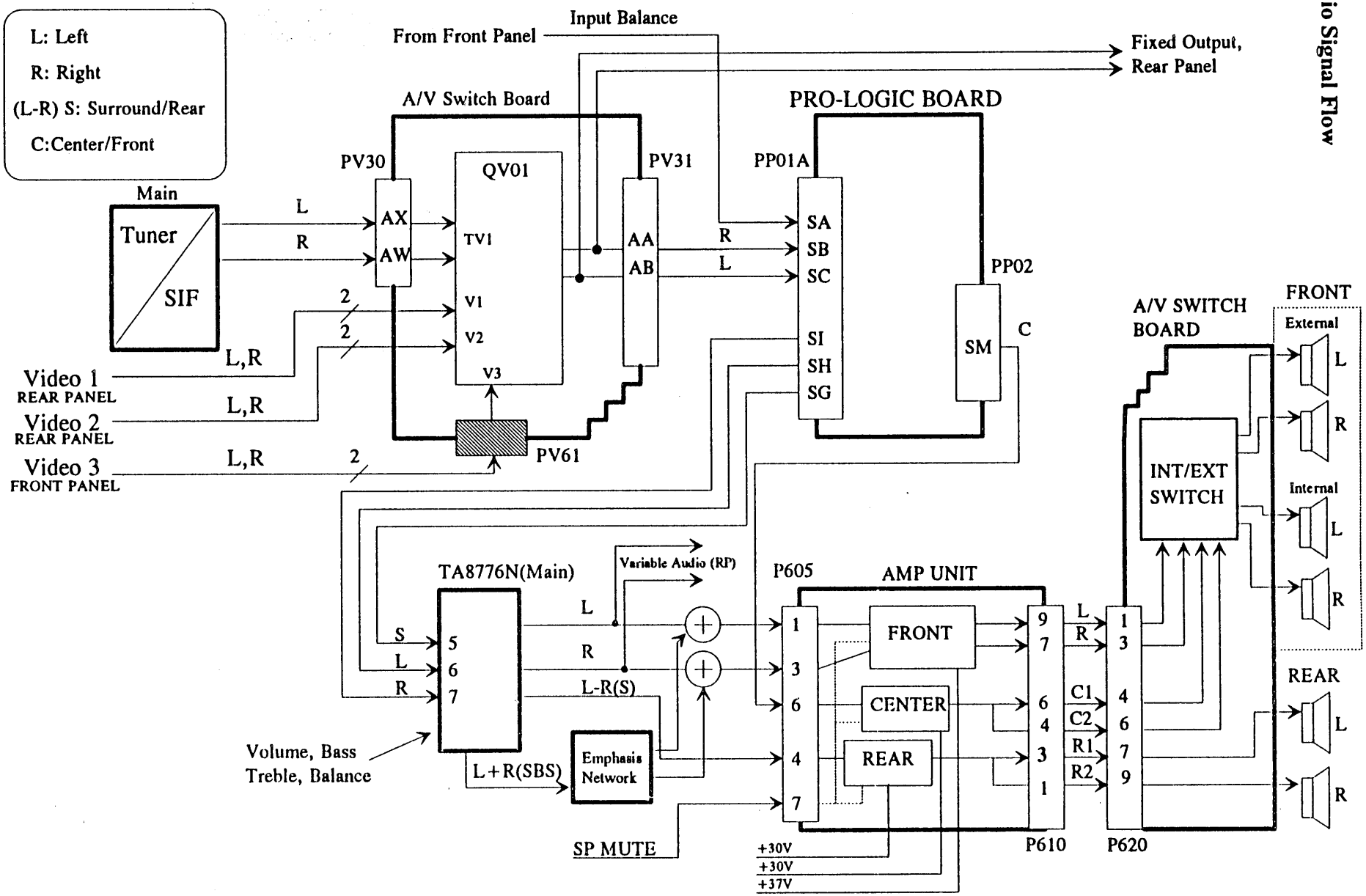
	Model Number	TP55C80 / TP55C81 / PJ55C80	TP48C90 / PJ48C90	TP48C70 / TP48C71	TP48C50 / TP48C51 / PJ48C50	TW56D90
GENERAL	Screen Size & CRT	55" Projection (4 : 3)	48" Projection (4 : 3)	48" Projection (4 : 3)	48" Projection (4 : 3)	56" Projection (16 : 9)
	Channel Capacity	181CH	181CH	181CH	181CH	181CH
	MTS with dbx	•	•	•	•	•
	SAP	•	•	•	•	•
	Remote Controls	Preprogram Univ. & EZ	Preprogram Univ. &EZ	Preprogram Univ.	Preprogram Univ.	Learn & EZ
	Number of Keys	45 & 7	45 & 7	44	42	51 & 7
	Picture-In-Picture	2 Tuner	2 Tuner	2 Tuner	1 Tuner	2 Tuner
	Projection Brightness	450 Ft L	600 Ft L	600 Ft L	600 Ft L	320 Ft .L
	Projection Viewing Angle	160°	160°	160°	160°	160°
SOUND	Dolby Surround	•	•	–	–	Pro-Logic
	Digital Sound Processor (DSP)	(4CH)	(4CH)	•	–	(4CH)
	Front Surround Sound	–	–	–	•	–
	Sub Bass System (SBS)	•	•	•	–	•
	Bass/Treble Control	•	•	•	•	•
	Number of Speakers	2+2	2+2	2	2	2 + 2
	Rear Speaker	•	•	–	–	•
	Audio output	28W+20W	28W+20W	28W	28W	28W + 20W + 20W
PICTURE	Comb Filter	Digital	Digital	Digital	CCD	3DY/C Separation
	Dynamic Quadruple Focus	•	•	•	•	•
	Velocity Scan Modulation	• (R.G)	• (R.G)	• (R.G)	• (R.G)	• (R.G.B)
	Black Level Expander	•	•	•	•	•
	Flesh Tone Control	•	•	•	•	•
	Dynamic Noise Reduction	•	•	•	•	•
	Picture Preference	•	•	•	•	•
	Horizontal Resolution	800 (S-IN)	800(S-IN)	800 (S-IN)	800 (S-IN)	900 (S-IN)
CONVENIENCE	Channel Return	•	•	•	•	•
	Parental Channel Lock	•	•	•	•	•
	Channel Caption	•	•	•	•	•
	3 Language Display	•	•	•	•	•
	Built-In Clock	•	•	•	•	•
	Closed Caption	•	•	•	•	•
TERMINALS	S-Video Input	1+1	1+1	1+1	1+1	1+1
	Audio/Video In/Out	2+1 In/1 Out	2+1 In/1 Out	2+1 In/1 Out	2+1 In/1 Out	2+1 In/1 Out
	Front Terminal	•	•	•	•	•
	Variable Audio Output	•	•	•	•	•
	2RF Input	•	•	•	–	•
	External Speaker Terminal	•	•	•	•	•

4. BLOCK DIAGRAMS

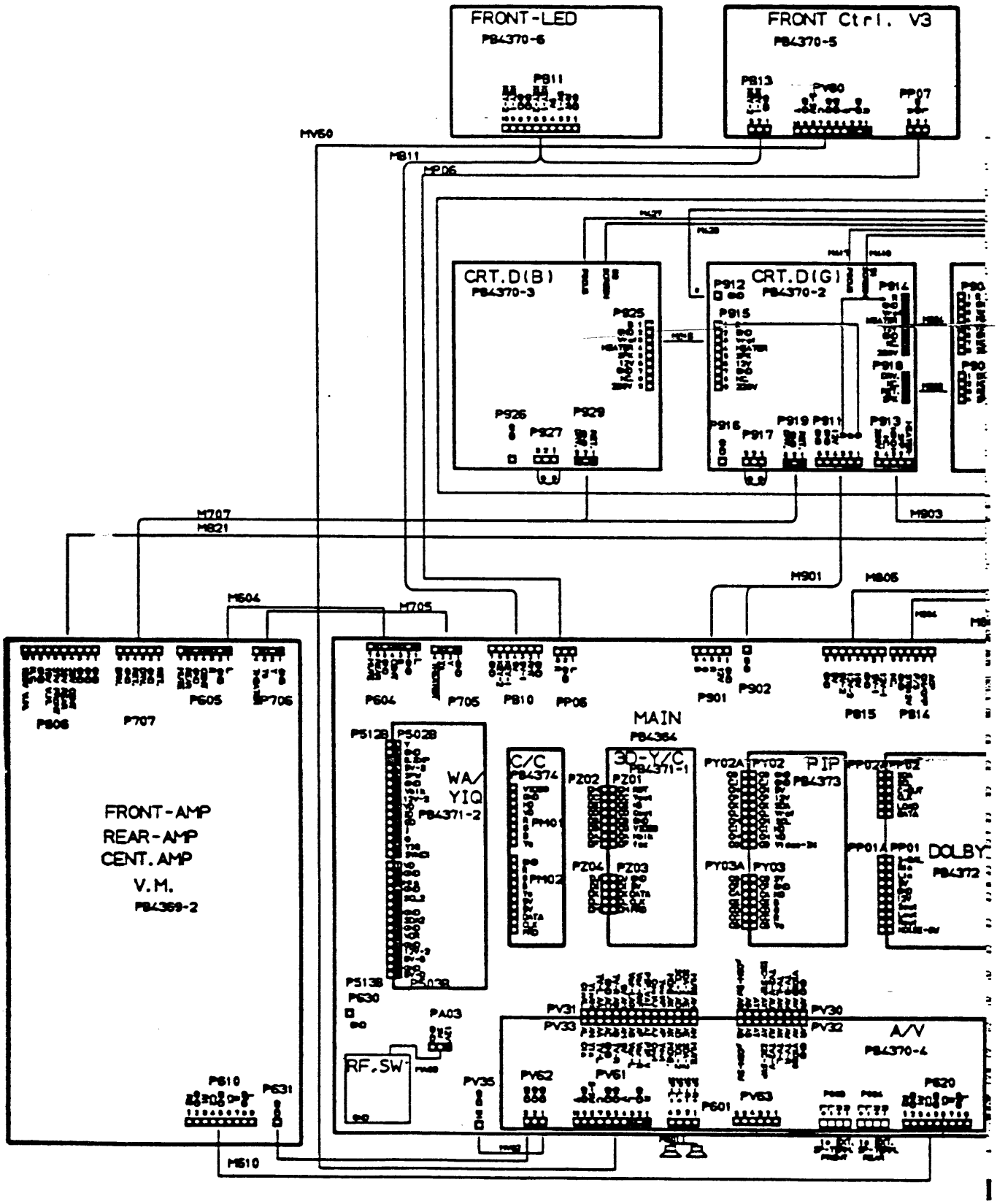
4-1. Video Signal Flow

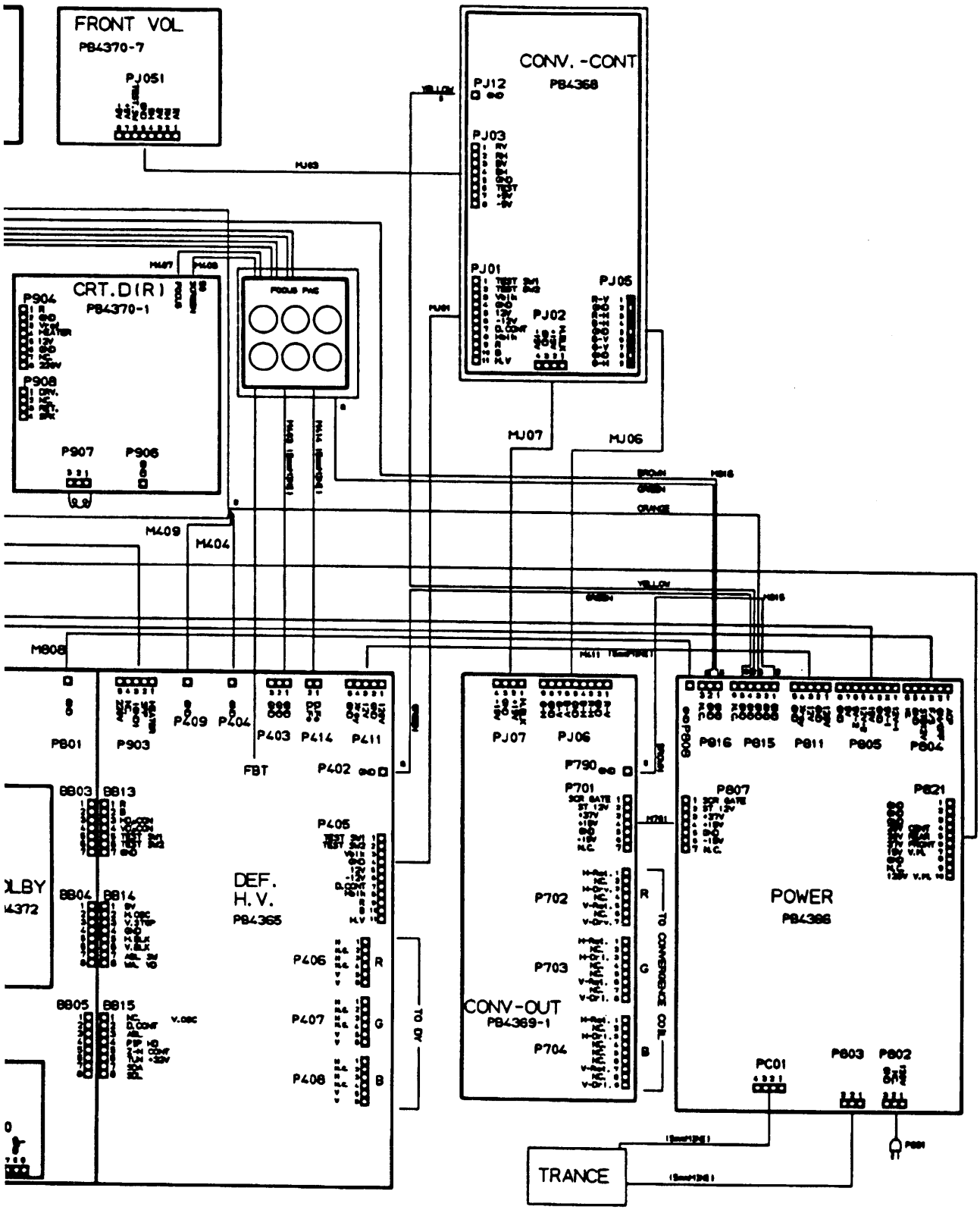


TW56D90 Audio Signal Flow Block Diagram



5. WIRING DIAGRAM




FRONT VOL
PB4370-7
PJ051
CONV. -CONT
PB4368
PJ12
PJ03
PJ01
PJ02
PJ05
CRT.D(R)
PB4370-1
P904
P908
P907
P906
MJ07
MJ06
M409
M404
M808
P801
P903
P409
P404
P403
P414
P411
FBT
P402
P405
P406
P407
P408
R
G
B
DEF.
H.V.
PB4365
P790
P701
P702
P703
P704
PJ07
PJ06
CONV-OUT
PB4369-1
P816
P815
P811
P805
P804
P807
P821
POWER
PB4366
PC01
P803
P802
TRANCE

SECTION II
WIDE ASPECT CIRCUIT

1. OUTLINE

A time compression IC (TC9078F) is used to display a picture image received on the current NTSC system, broadcasted in an aspect ratio of 4:3, onto a TV screen with an aspect ratio of 16:9. In displaying the picture, two modes are provided, namely, Standard and Wide.

This IC accepts as it's inputs digital Y and C signals, H and Y timing signals, performs a video signal time compression process, side panel insertion process H and V blanking restoration process. It also outputs various timing signals in addition to Y, I, Q analog (digital output is also available) signals and H, V drive signals.

Main features of TC9078F:

- Y signal processing in 1820fH, 10 bits to prevent degrading of DVCD D/C characteristics
- Memory, D/A equipped
- Responds to I^2C bus command structure
- Easy control

1-1. Standard Mode (4:3 Display)

In the standard mode, a picture with an aspect ratio of 4:3 is time-compressed by 3/4 in the horizontal direction and displayed on an arbitrary position of the wide screen having an aspect ratio of 16:9 so that it appears natural, not expanded.

Fig. 2-1 shows the screen picture display in the standard mode.

1-2. Wide, Full Mode (16:9 Display)

A picture with a 4:3 aspect ratio is not processed in the horizontal direction but is expanded in a vertical direction by the deflection system, and is then displayed. Vertical top and bottom areas of the picture are partially cut but the remaining part is expanded (zoomed) in a vertical direction to the aspect ratio of 16:9. Fig. 2-2 shows the picture display in the wide and full modes.

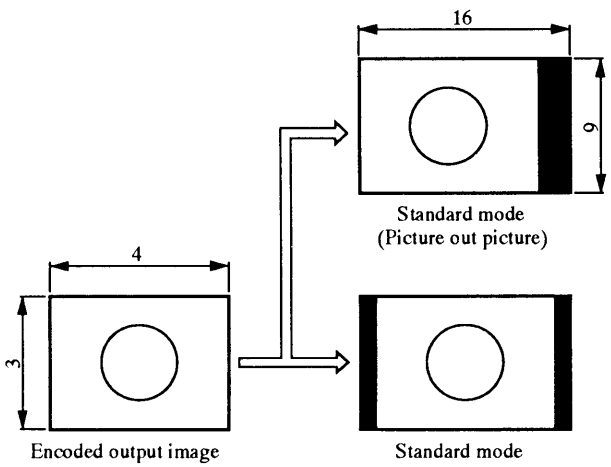


Fig. 2-1 The screen picture display in the standard mode

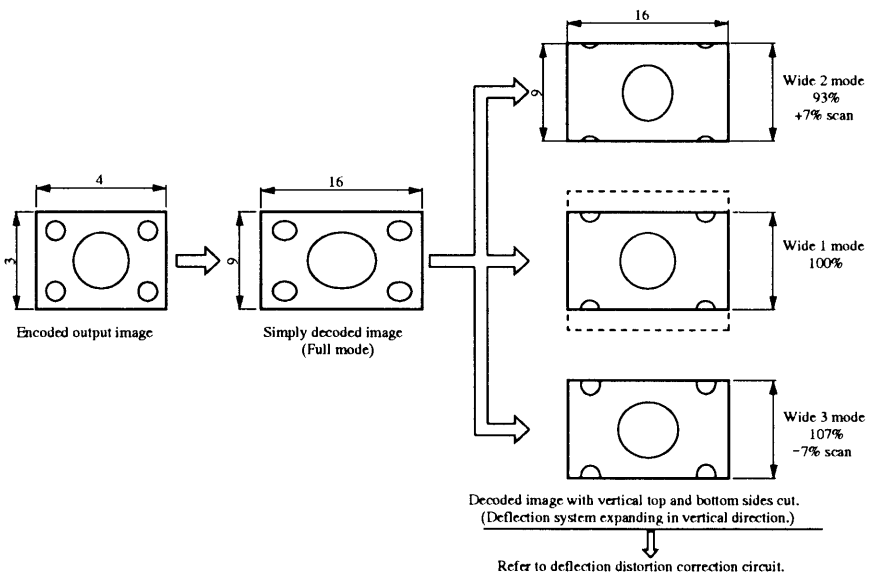


Fig. 2-2 Wide and Full mode picture display

2. BLOCK DIAGRAM

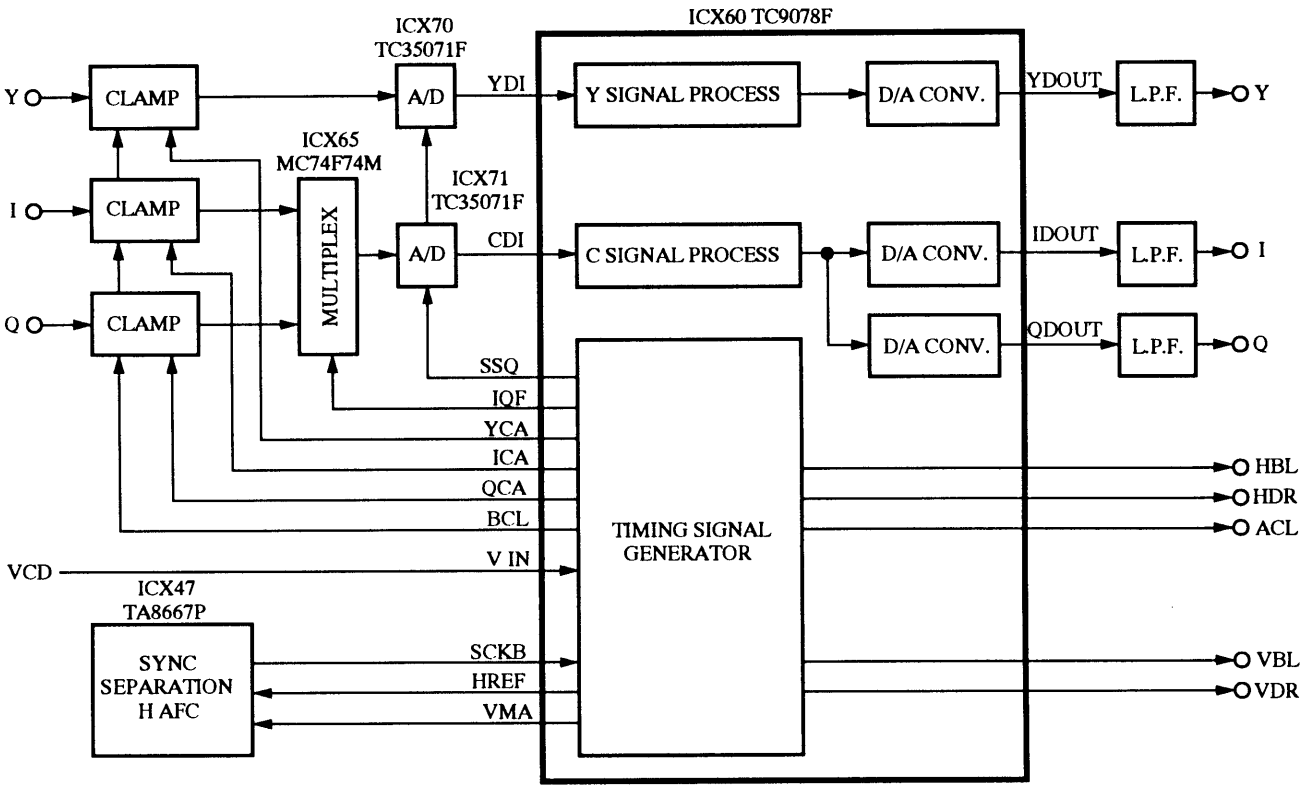


Fig. 2-3 TC9078F and peripheral circuits

A Toshiba TV H AFC IC "TA8667P" is used in the sync separation and H AFC circuit block. the TA8667P accepts HREF (reference signal for H PLL: signal developed by counting down SCKB into 1/2048) and VMA (V blanking mask signal for H PLL) from TC9078F, and generates a clock SCKB (2048fh system clock locked to H sync signal) and VIN (V sync signal) and sends them to TC9078F.

The Y signal and two components of the color signal, I and Q are fed to their respective clamp circuits. A BCL (prestage clamp signal) and YCA (Y input osffset cut pulse) are fed from TC9078F to the Y signal clamp circuit, and BCL and ICA (I input offset cut pulse) are fed to the I signal clamp circuit. Moreover BCL and QCA (Q input offset cut pulse) are fed to the Q signal clamp circuit. Each input is clamped and output with the offset controlled.

Two clamped color signals of I and Q are multiplexed in the IQ multiplex circuit by using IQF (I/Q phase signal) sent from TC9078F and the processed signal is fed to the C A/D converter as a C signal.

The A/D converter processes the Y signal and C signal by using SSQ (A/D clock) sent from WA.

TC9078F consists of a timing signal generation block, Y signal precess block, color signal process block, and three D/A converters. In the Y signal process block, the Y signal fed from the A/D converter is time compressed by 3/4 times in horizontal direction in the standard mode, but in the wide mode, the digital signal processed in 10 bits is converted and output as an analog signal without time compression. In the color signal process block, the C signal fed from the A/D converter is processed in the same way as in the Y signal process block and separated into each of I and Q signal. This signal is processed in 8 bits as a digital signal and the digital signal is converted and output as an analog signal.

3. DESCRIPTION OF ICs

3-1. System Configuration of ICX60 (TC9078F)

Fig. 2-4 shows entire configuration of the time compression IC ICX60 (TC9078F).

This IC consists of a Y signal process block, C signal process block, H system process block, V system process block, and I^2C bus decoder.

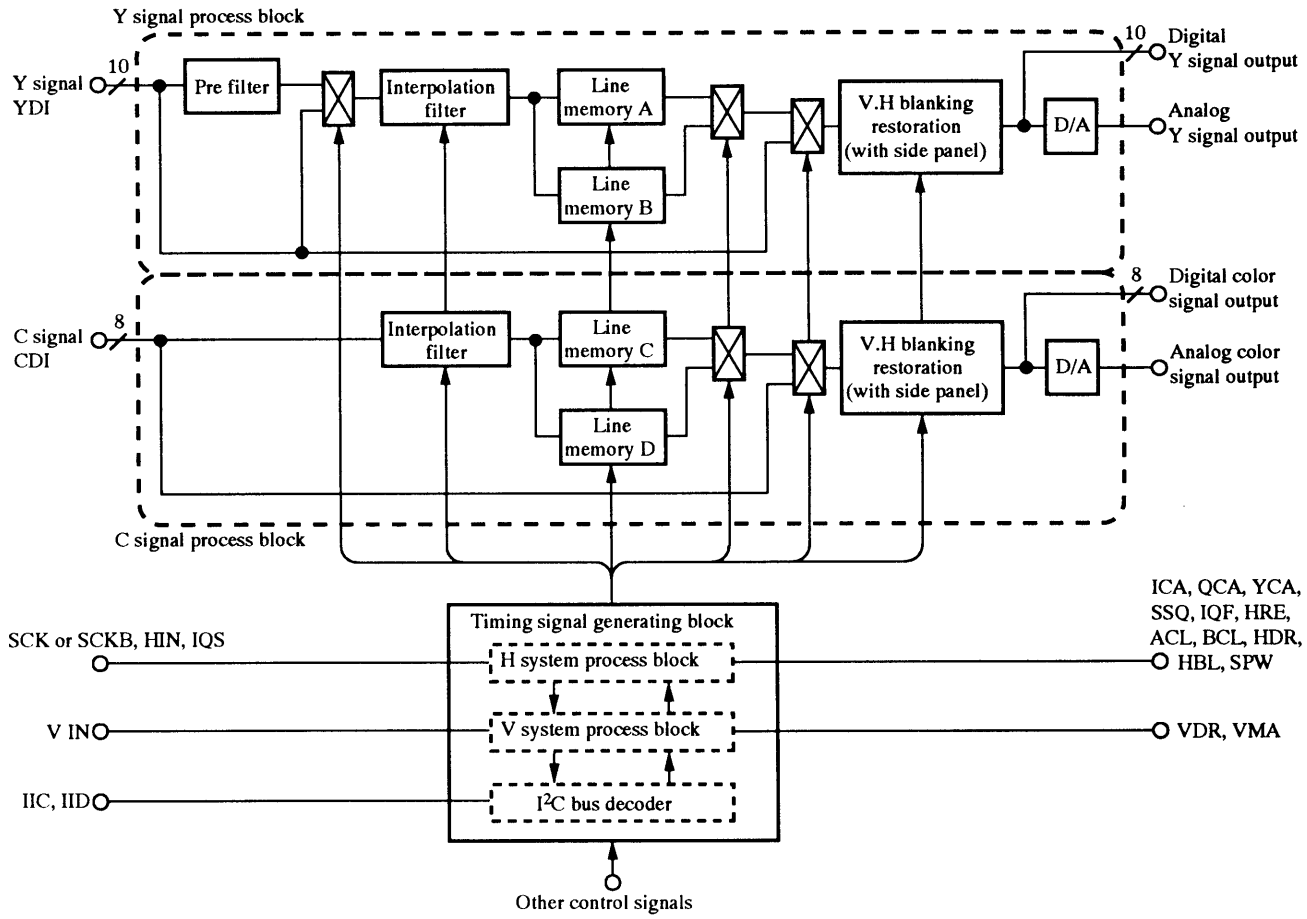


Fig. 2-4 System configuration of ICX60 (TC9078F)

3-1-1. Terminal Location Diagram of TC9078F (ICX60)

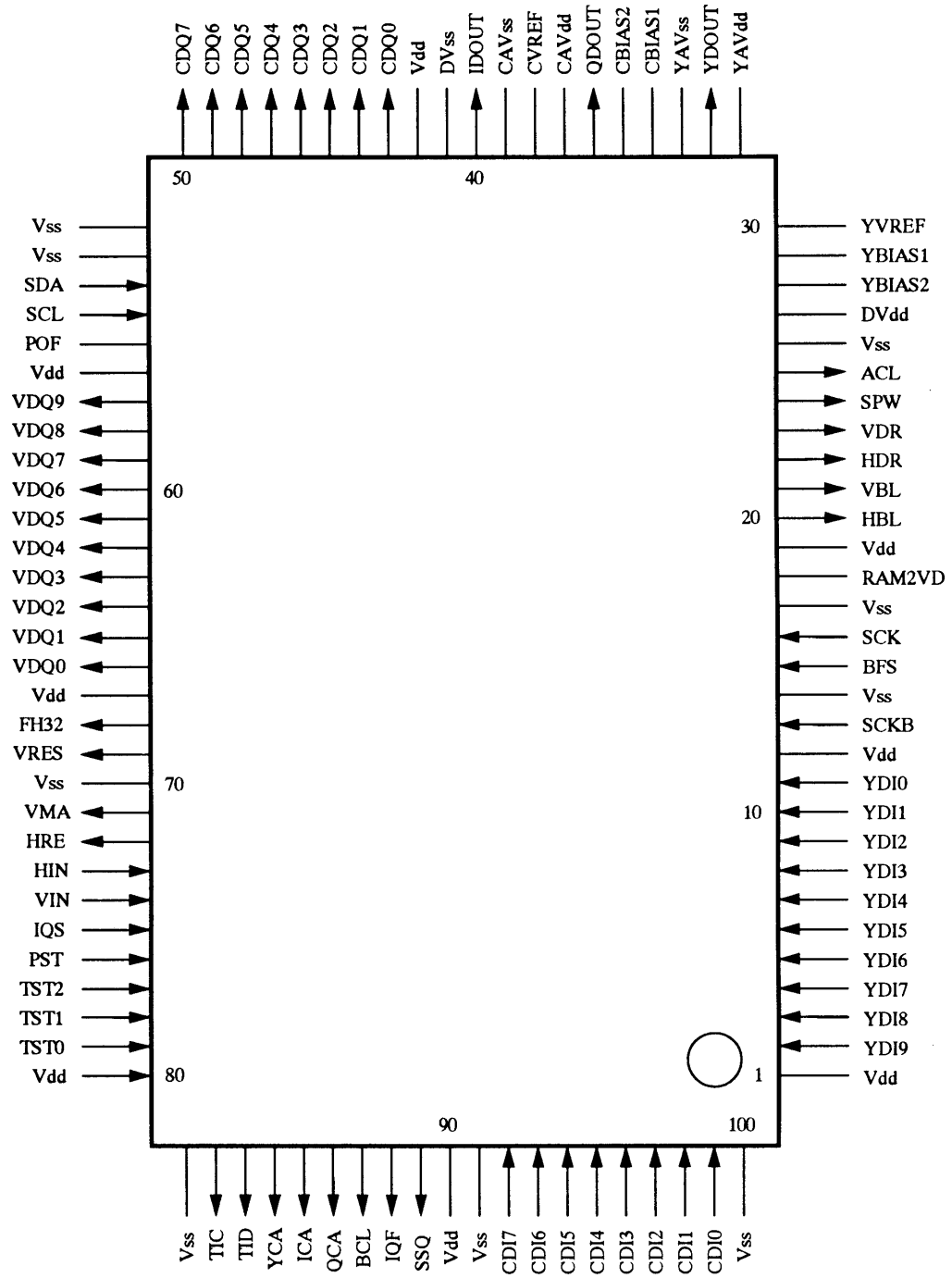


Fig. 2-5

3-1-2. Terminal Lists (1/2)

No.	Name	I/O	Function	Operating conditions
1	Vdd	–	Power supply 5V ±5% (for input buffer)	
2	YDI9	I	Y signal digital output (10 bit)	1024fH
3	YDI8	I	Y signal digital output (9 bit)	1024fH
4	YDI7	I	Y signal digital output (8 bit)	1024fH
5	YDI6	I	Y signal digital output (7 bit)	1024fH
6	YDI5	I	Y signal digital output (6 bit)	1024fH
7	YDI4	I	Y signal digital output (5 bit)	1024fH
8	YDI3	I	Y signal digital output (4 bit)	1024fH
9	YDI2	I	Y signal digital output (3 bit)	1024fH
10	YDI1	I	Y signal digital output (2 bit)	1024fH
11	YDI0	I	Y signal digital output (1 bit)	1024fH
12	Vdd	–	Power supply 5V ±5% (for DRAM/self bias input)	
13	SCKB	I	System clock (8fsc) self bias input	Input level: 1.5Vp-p
14	Vss		GND (for DRAM/self bias input)	
15	BFS	I	Clock input switch	SCKB input: GND
16	SCK	I	System clock (8fsc)	SCKB input: GND
17	Vss		GND (for output buffer)	
18	RAM2VD	–	1/2 Vdd (for DRAM)	
19	Vdd	–	Power supply 5V ±5% (for output buffer/internal logic)	
20	HBL	O	H blanking signal	
21	VBL	O	V blanking signal	
22	HDR	O	H drive trigger signal	
23	VDR	O	V drive trigger signal	
24	SPW	O	Velocity modulation ON/OFF control signal	
25	ACL	O	Later stage clamp signal	
26	Vss		GND (for internal logic)	
27	D-Vdd		Power supply 5V ±5% (Digital power supply for DAC)	
28	Y-BIAS2	–	Y output DAC bias terminal 2	
29	Y-BIAS1	–	Y output DAC bias terminal 1	
30	YVREF	I	Y output DAC reference	
31	A-Vdd		Power supply 5V ±5% (Analog power supply for Y-DAC)	
32	YDOUT	O	Y signal analog output	
33	A-Vss	–	GND (Y-DAC for analog power supply)	
34	CBIAS1		C output DAC bias terminal 1	
35	CBIAS1		C output DAC bias terminal 1	
36	QDOUT	O	Q signal analog output	
37	A-Vdd		Power supply 5V ±5% (Analog power supply for C-DAC)	
38	CVREF	I	C output DAC reference	
39	A-Vss		Power supply 5V ±5% (Analog power supply for C-DAC)	
40	IDOUT	O	I signal analog output	
41	D-Vss	–	GND (Digital power supply for DAC)	
42	Vdd	–	Power supply 5V ±5% (for output buffer/internal logic)	
43	CDQ0	O	C signal digital output (1 bit)	
44	CDQ1	O	C signal digital output (2 bit)	
45	CDQ2	O	C signal digital output (3 bit)	
46	CDQ3	O	C signal digital output (4 bit)	
47	CDQ4	O	C signal digital output (5 bit)	
48	CDQ5	O	C signal digital output (6 bit)	
49	CDQ6	O	C signal digital output (7 bit)	
50	CDQ7	O	C signal digital output (8 bit)	

3-1-3. Terminal Lists (2/2)

No.	Name	I/O	Function	Operating conditions
51	Vss		GND (for output buffer)	
52	Vss	–	GND (for internal logic)	
53	SDA	I/O	I^2C-bus data signal	
54	SCL	I	I^2C-bus clock signal	
55	POF	I	Power ON/OFF	Normal: High level
56	Vdd		Power supply 5V ±5% (for output buffer/internal logic)	
57	YDQ9	O	Y signal digital output	
58	YDQ8	O	Y signal digital output	
59	YDQ7	O	Y signal digital output	
60	YDQ6	O	Y signal digital output	
61	YDQ5	O	Y signal digital output	
62	YDQ4	O	Y signal digital output	
63	YDQ3	O	Y signal digital output	
64	YDQ2	O	Y signal digital output	
65	YDQ1	O	Y signal digital output	
66	YDQ0	O	Y signal digital output	
67	Vdd		GND (for output buffer)	
68	FH32	O	Test output	32fH
69	VRES	O	Test output	
70	Vss		GND (for input buffer)	
71	VMA	O	V blanking signal for H PLL	
72	HRE	O	H PLL reference signal	
73	HIN	I	H sync signal	
74	VIN	I	V sync signal	
75	IQS	I	Test input	Normal: GND
76	PST	I	Standard/non-standard switch signal	Standard: Low level
77	TST2	I	Test input	Normal: GND
78	TST1	I	Test input	Normal: GND
79	TST0	I	Test input	Normal: GND
80	Vdd		Power supply 5V ±5% (for input buffer)	
81	Vss		GND (for output buffer)	
82	TIC	O	Test output	
83	TID	O	Test output	
84	YCA	O	Y input system clamp level setting	
85	ICA	O	I input system clamp level setting	
86	QCA	O	Q input system clamp level setting	
87	BCL	O	Input system clamp pulse	
88	IQF	O	I/Q phase signal	
89	SSQ	O	For A/D clock output	1024fH
90	Vdd		Power supply 5V ±5% (for output buffer/internal logic)	
91	Vss		GND (for intrnal logic)	
92	CDI7	I		
93	CDI6	I	C signal digital input (7 bit)	
94	CDI5	I	C signal digital input (6 bit)	
95	CDI4	I	C signal digital input (5 bit)	
96	CDI3	I	C signal digital input (4 bit)	
97	CDI2	I	C signal digital input (3 bit)	
98	CDI1	I	C signal digital input (2 bit)	
99	CDI0	I	C signal digital input (1 bit)	
100	Vss		GND (for input buffer)	

3-2. H AFC IC, TA8667P (ICX47)

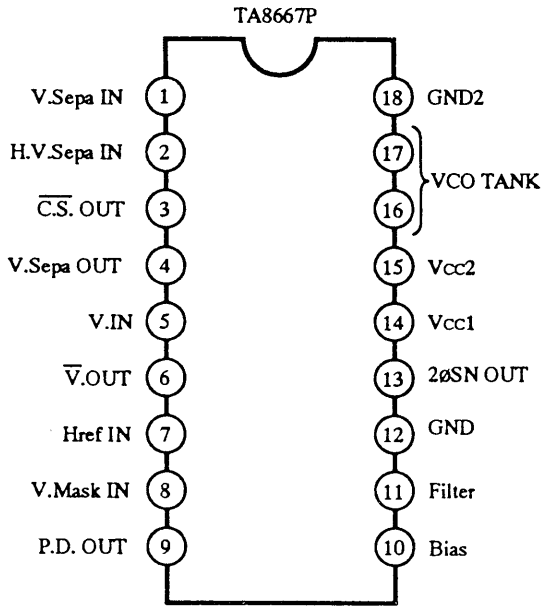


Fig. 2-6 Pin location diagram of TA8667P

Table 2-1 Pin discription of TA8667P

Pin No.	Pin name	Function
1	Vsepa IN	Video input terminal for V sync separation
2	Hsepa IN	Video input terminal for H sync separation
3	CS-OUT	C sync output terminal
4	Vsepa OUT	SYNC output terminal for V sync separation
5	V-IN	V sync separation input terminal
6	V-OUT	V-SYNC output terminal
7	Href IN	H reference pulse input terminal
8	VMask IN	AFC operation mask signal input terminal
9	PD OUT	Phase comparison result output terminal
10	Bias	fo voltage output terminal
11	filter	VCO control voltage input terminal
12	GND1	Ground
13	2øSN OUT	Clock output
14	Vcc 1	Power supply +9V
15	Vcc 2	Power supply +9V
16	VCO TANK	Tank coil connection terminal
17	VCO TANK	Tank coil connection terminal
18	GND2	Ground

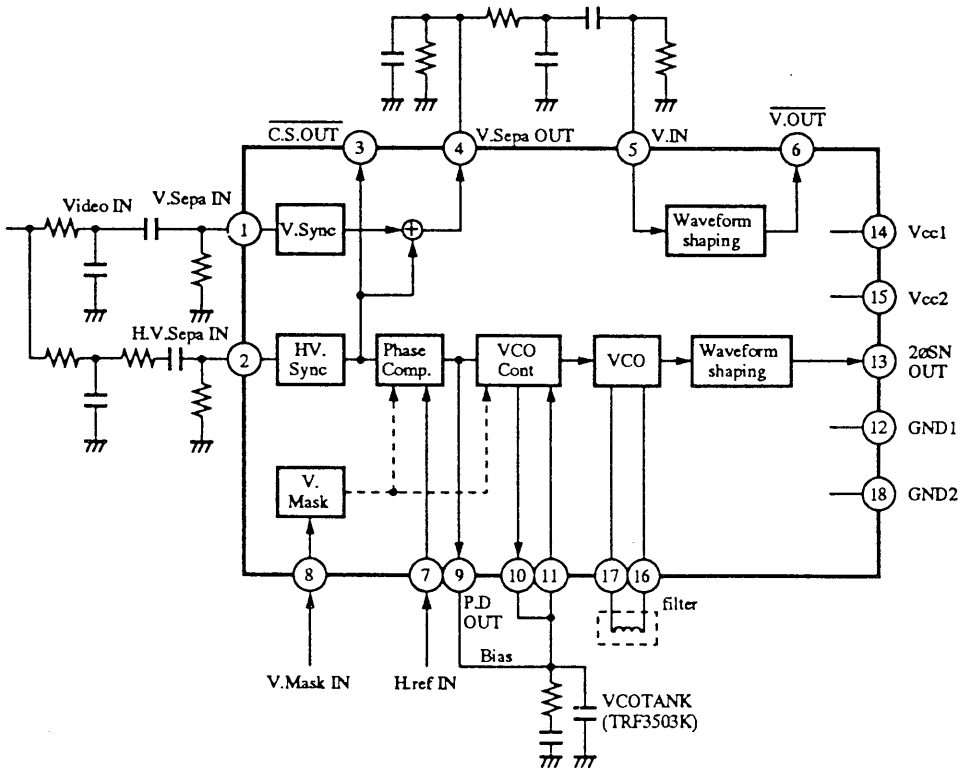


Fig. 2-7 Block diagram of TA8667P

3-3. Deflection Distortion Correction Circuit

3-3-1. Deflection Distortion Correction IC (TA8859P), IC360

(1) Outline

The deflection distortion correction IC (TA8859P) in combination with a V/C/D IC (TA8859) having a vertical pulse output signal can perform various deflection distortion corrections and V output correction through the I^2C bus control.

The I^2C bus controls are carried out by the microcomputer and can controlled with a remote control.

(2) Functions and features

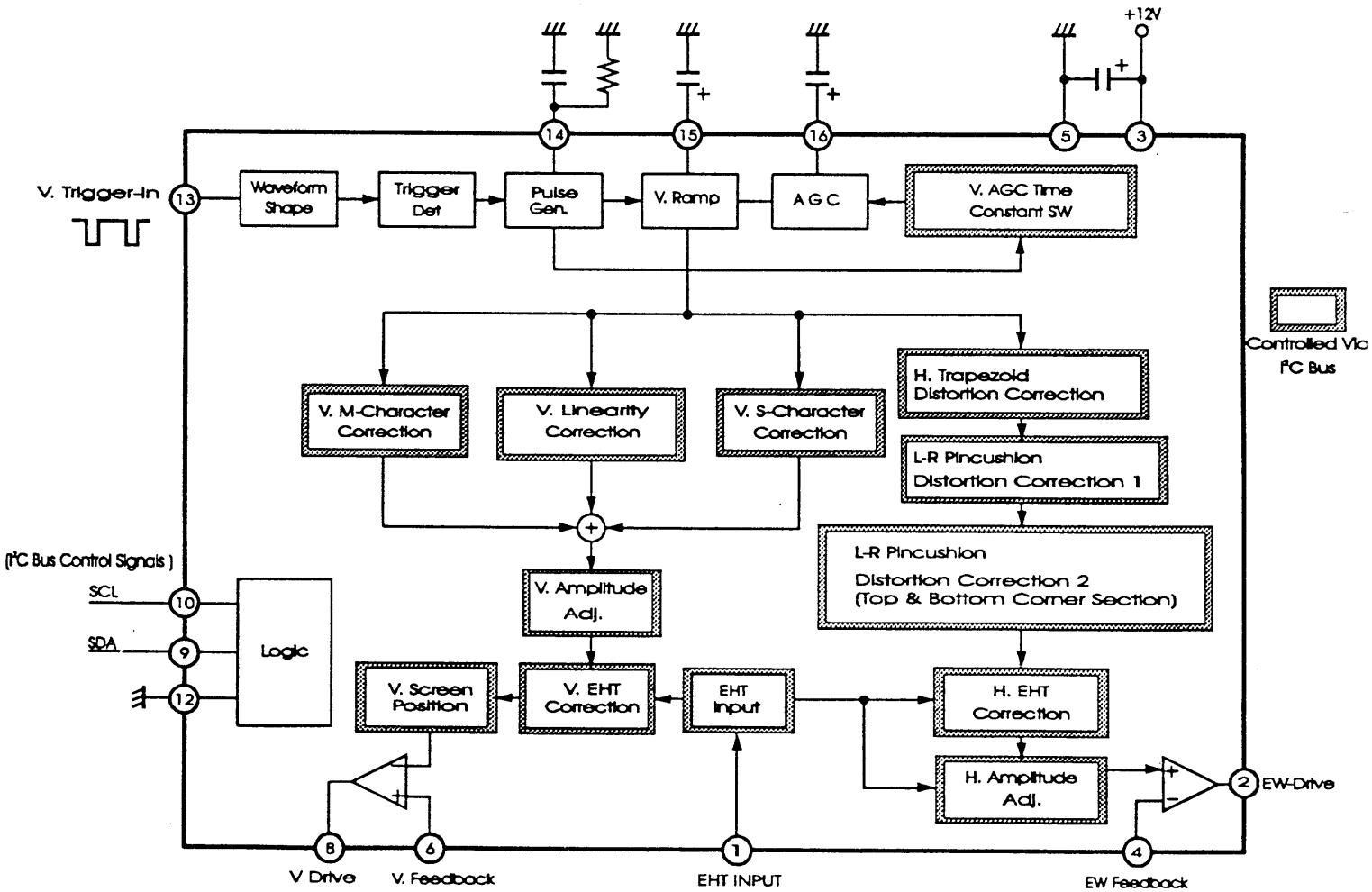
TA8859P contains various functions such as V ramp voltage generation, V amplitude automatic switching (50/60 Hz), V linearity correction, V amplitude amplification, EHT correction, I^2C bus control interface, and controls following items through the I^2C bus.

(1) V amplitude (Standard, WIDE1, WIDE2, WIDE3)
(2) V linearity
(3) V S-character correction
(4) V screen position (center voltage setting)
(5) V M-character correction
(6) V EHT correction
(7) V AGC time constant switching

(3) Circuit/Block diagram

Fig. 2-10 shows a basic block diagram.

Fig. 2-10 Block diagram of TA8859P



SECTION III
3-DIMENSION Y/C SEPARATION CIRCUIT

1. OUTLINE

1-1. Motion Response 3 Dimensional Y/C Separation

3 dimensional Y/C separation is carried out by a comb filter with a frame memory and exhibitss ideal separation characteristics. Clearer pictures without cross color and dot interference are obtained for still pictures.

1-1-1. Motion Response Y/C Separation System

(1) 2 dimensional Y/C separation

A color sub carrier signal fsc in the NTSC system has the following relationship with the H scanning frequency fH.

$$fsc = \frac{455}{2} \cdot f_H \ (= 3.58MHz)$$

This means that the phase of the color signal is inverted every scanning line as shown in Fig. 3-1. Accordingly, the Y/C separation is accomplished by performing addition and subtraction for the signals corresponding to upper and lower scanning lines. Fig. 3-2 shows this concept. That is, the color signal is cancelled by adding the signals for the upper and lower scanning lines and the Y signal is cancelled by subtracting. As a result, each separated output is obtained.

In lower priced or older televisions, one dimensional Y/C separation is carried out by using a 3.58 MHz band pass filter. This separation system which utilizes a correlation in the upper and lower directions is termed 2 dimensional Y/C separation.

In this system, slanted stripes are processed as a color signal and cross color occurs. That is, for signals of which hue varies sharply in the vertical direction, the sharpened area appears as a Y signal and causes undesirable problems such as an edge dot interference.

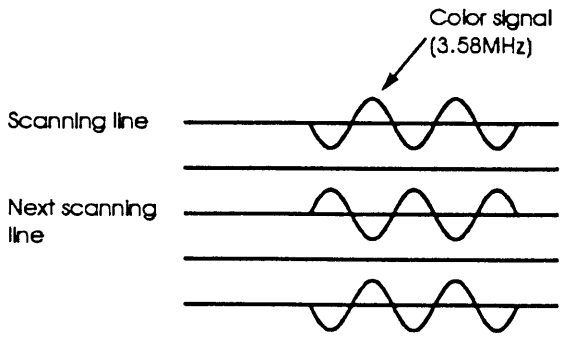


Fig. 3-1 Frequency interleaving

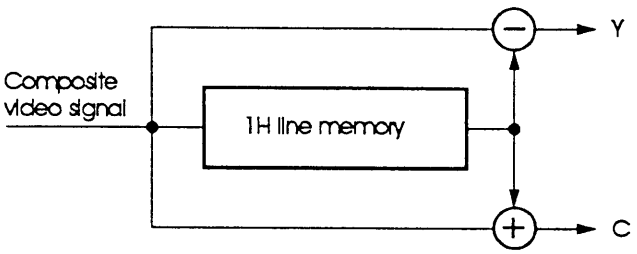


Fig. 3-2 2 dimensional Y/C separation

(2) 3 dimensional Y/C separation

In the NTSC system, the scanning lines in the same phase move upwards by one scanning line per field (Fig. 3-3). That is, as the phase of the C signal is inverted every frame, the Y signal or the C signal is separated by using addition or subtraction with the same pixel from the preceeding frame.

Fig. 3-4 shows a model of this operation. In this case, the signal in the previous frame is used and the ideal Y/C separation is available for a still picture. However, for a motion picture, the separation process is carried out with the picture moved before 1/30 sec, thus causing a defect showing no separation.

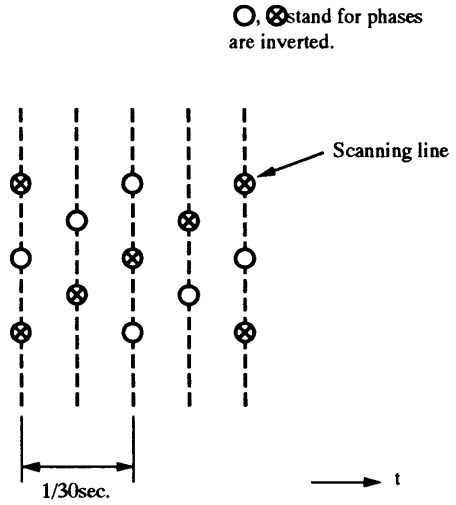


Fig. 3-3 Structure of scanning lines

(3) Motion response type Y/C separation

If the 2 dimensional Y/C separation system or the 3 dimensional Y/C separation system stated previously is switched according to the presence of motion, the defects of both systems are compensated and optimum Y/C separation will be obtained. In this system, the performance is determined by the accuracy of motion detection and the setting of a mixing ratio which will allow smooth switching.

Fig. 3-5 shows a block diagram of this circuit.

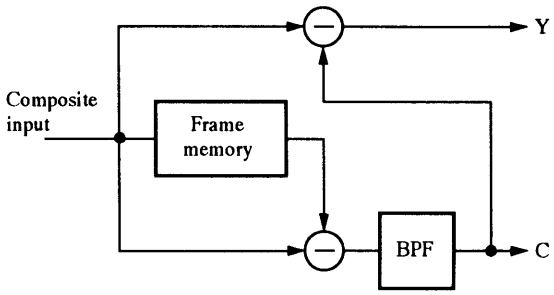


Fig. 3-4 Three dimensional Y/C separation circuit

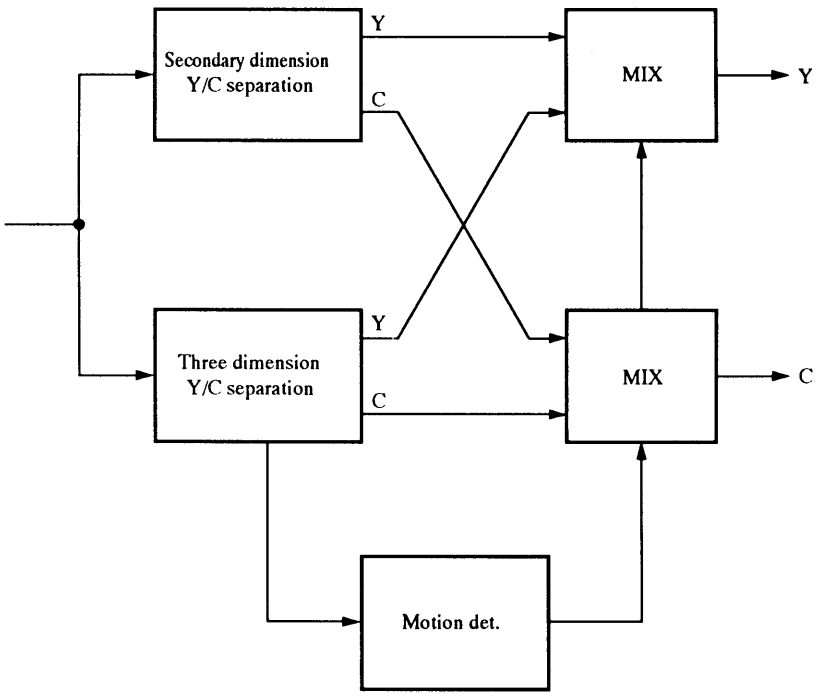


Fig. 3-5 Motion response Y/C separation circuit

1-1-2. Motion Response 3 Dimensional Y/C Separation Process Block

The motion response 3 dimensional Y/C separation is carried out with ICZ01 and a field memory (ICZ06, ICZ07) used as a frame delay. The video signal is digitized by ICZ03 (A/D) enters ICZ01. The decision of whether the image is a motion picture or a still picture is carried out by comparing the video signal with a frame delayed signal, MDI0–7, respectively. The picture area determined to be a still picture is Y/C separated with a frame type comb filter and the picture area determined to be a motion picture is Y/C separated with a line type comb filter.

However, this 3 dimensional Y/C separation is carried out for the standard signals only. Identification of the standard signal is carried out inside ICZ01. See Service Data P/N 050-737 schematics page 5/6 for the actual circuit diagram.

2. DESCRIPTION OF IC's

2-1. GENERAL

Specific information for IC's located on the 3D Y/C Board can be found in Service Data P/N 050-737, pages 96-98. On the following page, however, table 3-1 contains information regarding pinouts and signal descriptions for ICZ01 (TC9057AF).

Table 3-1 TC9057AF, YCII Pin List

Pin	Name	Function
1	RCK	Field-Memory READ CK
2	WCK	Field-Memory WHITE CK
3	VMASK	V mask
4	HREF	H AFC reference
5	VMI	V sync
6	HCS	Composite sync
7	Vdd	[DRAM]
8	FS2N	1820fH-CK
9	Vss	[DRAM]
10	FS	4fsc-CK
11	Vss	
12	SDATA	PLL, CLAMP serial DATA
13	SCLOCK	PLL, CLAMP serial DATA clock
14	LATCH	PLL, CLAMP serial DATA latch pulse
15	RESET	IC TEST
16	TEST1	IC TEST
17	TEST2	IC TEST
18	PERIOD	T-bus (latch pulse)
19	CLOCK	T-bus (clock)
20	DATA	T-bus (DATA)
21	Vdd	
22	PLLERR	PLL error DATA
23	HCRES	H counter/reset
24	CBFP	Burst flag pulse
25	ACP1	Clamp pulse
26	STD	Standard ID
27	DNK	Motion signal
28	AGCDET	AGC or 2F Det OFF
29	KILL	Color killer
30	CKOUT	CK output (positive logic)
31	DVS7	NTSC or SVHS-Y inuput (MSB)
32	DVS6	NTSC or SVHS-Y inuput
33	DVS5	NTSC or SVHS-Y inuput
34	DVS4	NTSC or SVHS-Y inuput
35	DVS3	NTSC or SVHS-Y inuput
36	DVS2	NTSC or SVHS-Y inuput
37	DVS1	NTSC or SVHS-Y inuput
38	DVS0	NTSC or SVHS-Y inuput (LSB)
39	DKOFF	1F-det. OFF (MUSE-DC)
40	YOUT0	Y signal output (LSB)
41	YOUT1	Y signal output
42	YOUT2	Y signal output
43	YOUT3	Y signal output
44	YOUT4	Y signal output
45	YOUT5	Y signal output
46	YOUT6	Y signal output
47	YOUT7	Y signal output
48	YOUT8	Y signal output
49	YOUT9	Y signal output (MSB)
50	Vss	

Pin	Name	Function
51	COUT0	C signal output (LSB)
52	COUT1	C signal output
53	COUT2	C signal output
54	COUT3	C signal output
55	COUT4	C signal output
56	COUT5	C signal output
57	COUT6	C signal output
58	COUT7	C signal output
59	COUT8	C signal output
60	COUT9	C signal output (MSB)
61	Vdd	
62	DACKOUT	CK output (negative logic)
63	Vss	
64	MAI3	Field-Memory A input (MSB)
65	MAI2	Field-Memory A input
66	MAI1	Field-Memory A input
67	MAI0	Field-Memory A input (LSB)
68	MAO3	Field-Memory A output (MSB)
69	MAO2	Field-Memory A output
70	MAO1	Field-Memory A output
71	MAO0	Field-Memory A output (LSB)
72	Vss	
73	MBI3	Field-Memory B input (MSB)
74	MBI2	Field-Memory B input
75	MBI1	Field-Memory B input
76	MBI0	Field-Memory B input (LSB)
77	MBO3	Field-Memory B output (MSB)
78	MBO2	Field-Memory B output
79	MBO1	Field-Memory B output
80	MBO0	Field-Memory B output (LSB)
81	MCI3	Field-Memory C input (MSB)
82	MCI2	Field-Memory C input
83	MCI1	Field-Memory C input
84	MCI0	Field-Memory C input (LSB)
85	MCO3	Field-Memory C output (MSB)
86	MCO2	Field-Memory C output
87	MCO1	Field-Memory C output
88	MCO0	Field-Memory C output (LSB)
89	Vdd	
90	Vdd	
91	MDI3	Field-Memory D input (MSB)
92	MDI2	Field-Memory D input
93	MDI1	Field-Memory D input
94	MDI0	Field-Memory D input (LSB)
95	MDO3	Field-Memory D output (MSB)
96	MDO2	Field-Memory D output
97	MDO1	Field-Memory D output
98	MDO0	Field-Memory D output (LSB)
99	RSTR	Field-Memory READ reset
100	RSTW	Field-Memory WRITE reset

MEMO

SECTION IV
DOLBY PROLOGIC CIRCUIT

1. DOLBY PROLOGIC CIRCUIT OUTLINE

1-1. Origins of Dolby Surround

Dolby Stereo movies and Dolby Surround video and television programs include an additional sonic dimension over conventional stereo productions. They are made using a Dolby MP (Motion Picture) Matrix encoder, which combines four channels of audio into a standard two-channel format, suitable for recording or transmitting the same as regular stereo programs.

To recapture the dimensional properties brought by the additional channels, a Dolby Surround decoder is used. In the theater, a professional decoder is part of the Dolby Stereo cinema processor used to play 35 mm stereo optical prints. The decoder recovers the left, center, and right signals for playback over three front speakers, and extracts the surround signal for distribution over an array of speakers wrapped around the sides and back of the theater. (These same speakers may also be driven from four of the six discrete tracks on 70 mm Dolby Stereo magnetic prints, but in this case no decoder is needed.)

Home viewing of movies on video has become extremely popular, and with the advent of stereo VCR's, stereo television and digital video discs, the audio side of the video presentation has improved considerably, inviting the use of full-range sound reproduction. The ability to deliver high quality audio in these formats made it easy to bring MP Matrix-encoded soundtracks into the home as well, thus establishing the foundation for Dolby Surround.

1-2. The Dolby MP Matrix

One of the original goals of the MP Matrix was to enable Dolby Stereo soundtracks to be successfully played in theaters equiped for mono or two-channel stereo sound. This allows movies to be distributed in a single optical format, and furtheremore results in complete compatibility with home video media without requiring separate soundtrack mixes. Since the three front channels of the MP Matrix are assembled in virtually the same way as a conventional stereo mix – left into left, center equally into left and right, and right into right – playing a Dolby Stereo soundtrack over two speakers reproduces the entire encoded soundtrack. There is but one exception: the surround signal, though audible, is not reproduced in its proper spatial perspective. When the first home decoder was developed in 1982, its goal was to restore this lone missing dimension.

Before we discuss decoders, it is necessary to see how the MP Matrix encoder works. Referring to the conceptual diagram in Fig. 4-1, the encoder accepts four separate input signals; left, center, right, and surround (L, C, R, S), and creates two final outputs, left-total and right-total (Lt and Rt).

The L and R inputs go straight to the Lt and Rt outputs without modification, and the C input is divided equally to Lt and Rt with a 3 dB level reduction (to maintain constant acoustic power). The S input is also divided equally between Lt and Rt, but it first undergoes three additional processing steps:

- Frequency bandlimiting from 100 Hz to 7 kHz.
- Encoding with a modified from of Dolby B-type noise reduction.
- Plus and minus 90-degree phase shifting is applied to create a 180-degree phase differential between the components feeding Lt and Rt.

It is clear there is no loss of separation between the left and right signals; they remain completely independent. Not so obvious is that there is also no theoretical loss of separation between the center and surround signals. Since

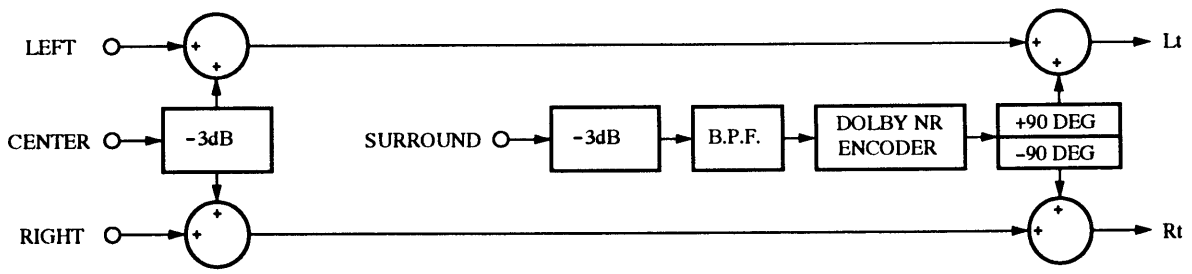


Fig. 4-1 Conceptual Dolby Stereo/Dolby Surround encoder

the surround signal is recovered by taking the difference between Lt and Rt, the identical center channel components in Lt and Rt will exactly cancel each other in the surround output. Likewise, since the center channel is derived from the sum of Lt and Rt, the equal and opposite surround channel components will cancel each other in the center output.

The ability for this cancellation technique to maintain high separation between center and surround signals requires the amplitude and phase characteristics of the two transmission channels to be as close as possible. For instance, if the center channel components in Lt are not identical to the ones in Rt as a result of a channel balance error, center information will come out of the surround channel in the form of unwanted crosstalk.

1-3. The Dolby Surround Decoder

This leads us to the original Dolby Surround decoder. The block diagram in Fig. 4-2 shows how the decoder works. Except for level and channel balance corrections, the Lt input signal passes unmodified and becomes the left output. The Rt input signal likewise becomes the right output. Lt and Rt also carry the center signal, so it will be heard as a "phantom" image between the left and right speakers, and sounds mixed anywhere across the stereo soundstage will be presented in their proper perspective. The center speaker is thus shown as optional since it is not needed to reproduce the center signal.

The L-R stage in the decoder will detect the surround signal by taking the difference of Lt and Rt, then passing it through a 7 kHz low-pass filter, a delay line, and complementary Dolby noise reduction. The surround signal will also be reproduced by the left and right speakers, but it will be heard out-of-phase which will diffuse the image.

Since the heart of the decoding process is a simple L-R difference amplifier, it is referred to generically as a "passive" decoder. This is to distinguish it from decoders using active processes to enhance separation which are known as "active" decoders.

1-4. Prologic Decoding

Today, audio/video systems have taken on new dimensions; televisions with 26-inch picture sizes are popular, with a move toward even larger screens underway. Rear projection sets from 40 to 60 inches are becoming mainstream products, as are projection systems with 6- to 12-foot screens. Larger screens and increased video resolution bring the home viewer more of the movie theater experience, and benefit greatly from expanded sonic dimensions to balance the presentation. These factors led to Dolby's introduction of Prologic, the second generation in Dolby Surround decoding technology.

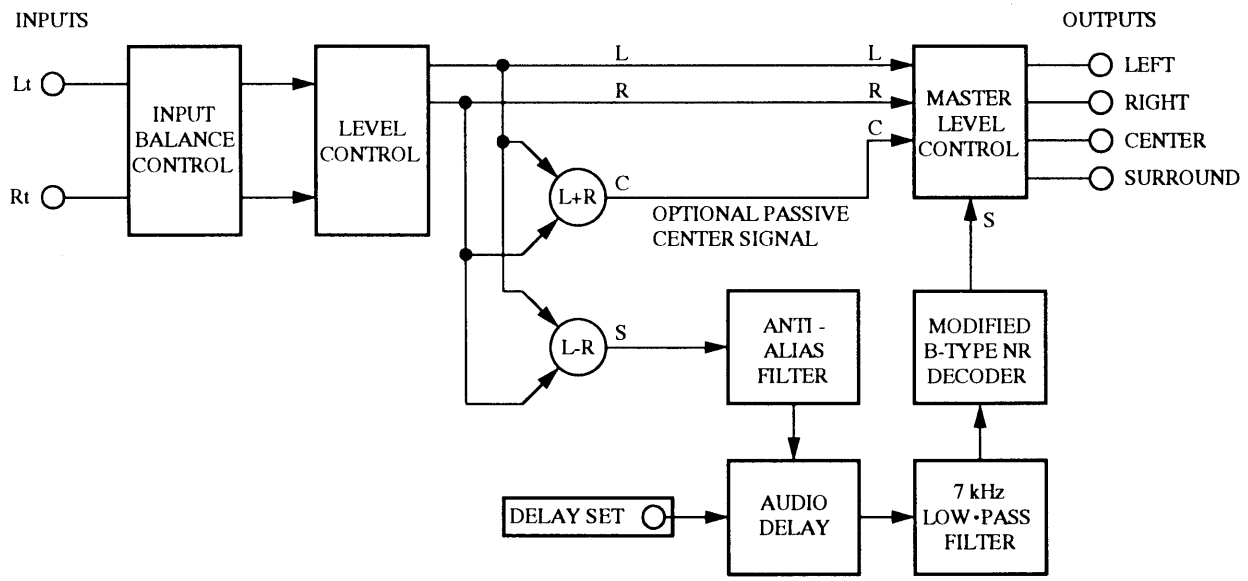


Fig. 4-3 Prologic decoder block diagram

Prologic is an active process designed to enhance sound localization through the use of high-separation decoding techniques. The system is a direct descendant of the one used in Dolby Stereo cinema processors, featuring a center channel output to complement the left, right, and surround channels.

1-5. Concept of Active Decoding Directional Enhancement

Passive decoders, use a simple differential stage to extract the surround signal from the left and right input signals. The decoders maintain high channel separation across the front, but localization is proper only within a particular seating area where the phantom-center image is optimal. Furthermore, even with the effects of additional surround channel processing, it is not possible to obtain a total degree of isolation from front to back since the surround speakers reproduce any difference information in the Lt/Rt composite. Due to these factors, passive decoders are limited in their ability to place sounds with ultimate precision for all viewing positions.

Active decoders employ directional enhancement techniques which attempt to remove matrix system crosstalk by manipulating the output signals of the decoder. Their goal is to create sharply focused sound images and to recreate directional cues over a wide listening area. An active decoder can most easily be thought of as a passive decoder followed by an enhancement circuit.

1-6. Prologic Adaptive Matrix

Just as the LR differential stage is the heart of a passive decoder, the adaptive matrix is the heart of a Prologic decoder. Two main signals go in (Lt and Rt), and four resultant signals emerge (L, C, R, and S). Compare the block diagram of the Prologic decoder in Fig. 4-3 with the passive decoder in Fig. 4-2. Except for the matrix stage (and some ancillary circuits), they are virtually the same.

To summarize, Prologic operates by continuously monitoring the encoded soundtrack, evaluating the inherent soundfield dominance, and applying enhancement in the same direction and in proportion to that dominance. To see how the circuit works, we will examine the block diagram in Fig. 4-4

otice the decoder employs two parallel paths: a relatively direct audio path and a complex control path. Most of the decoder's electronics are used to condition and analyze the input signals rather than to actually process the audio itself.

As you may guess, the main order of business is to generate the signal dominance vector. The first step in this process is to condition the incoming signals to prevent decoder errors. This is done by bandpass filtering the Lt and Rt signals in the control path to strip off low-frequency signals which do not provide directional

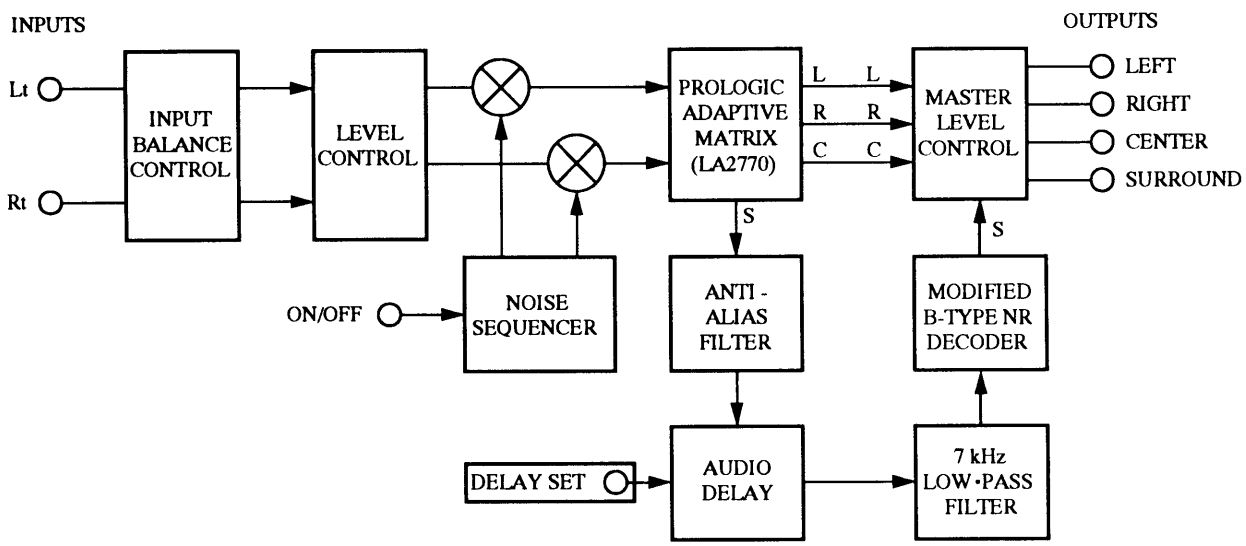


Fig. 4-3 Prologic decoder block diagram

cues, and to attenuate high frequencies that may contain uncertain phase or amplitude characteristics.

The next step is to determine the magnitudes of the two orthogonal signal paris, which is done by first full-wave rectifying each cardinal signal, subjecting the resulting DC voltages in pars to log conversion, then taking their difference. Two independent control signals are now available; one representing dominance along the left/right axis, the other along the center/surround axis.

Even though there are only two control voltages at this point, they are of dual polarity, or bipolar. For instance, when the left/right voltage deflects upward, the dominance is to the left; when it goes downward, the dominance is to the right. At the midpoint, no dominance is indicated. Each of these control voltages is evaluated continuously to determine if their relative dominance exceeds a certain threshold point. If either does, the control circuit switches to the fast mode.

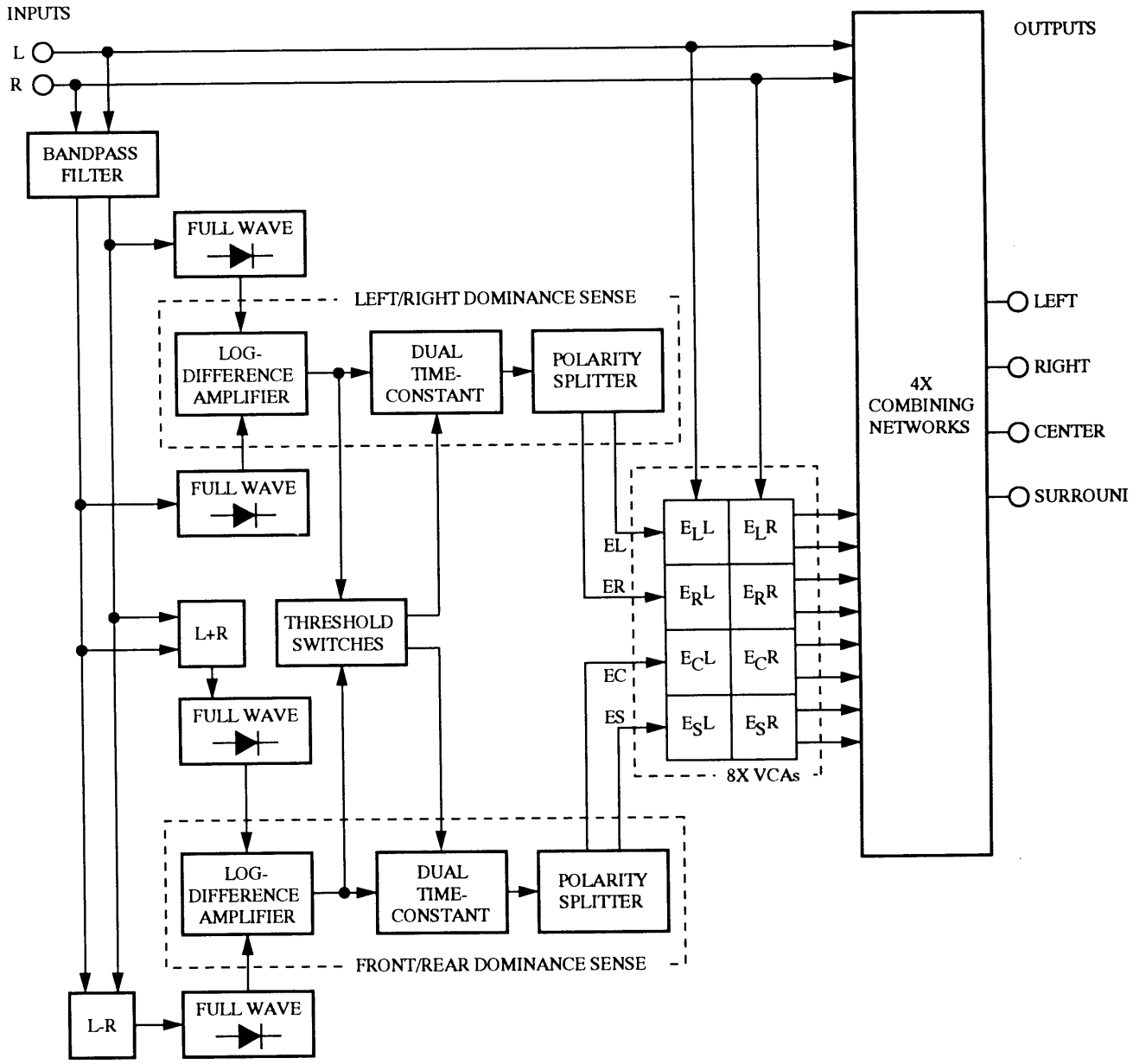


Fig. 4-4 Prologic adaptive matrix

A polarity splitter resolves the two bipolar dominance signals into four unipolar control voltages, called EL, ER, EC, and ES. The now reflect soundtrack dominance in electrical terms embodying psychoacoustic properties, and so are ready to be applied to the signal-canceling VCA stages. Since there are two input channels (lt and Rt) and four control voltages, eight VCAs are used to generate eight variable sub-terms. When added with the Lt and Rt inputs, ten individual terms are available. To construct a decoded output signal, portions of each of the ten terms are added or subtracted with a predetermined weighting factor in the combining networks. Use of the appropriate magnitudes and signs for the forty summed components gives the desired directional enhancement and non-dominant signal redistribution, all the while maintaining constant acoustic power for the signal components.

Fig. 4-5 Prologic decoder separation map

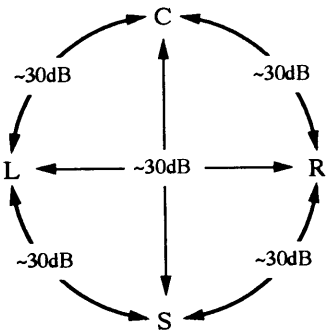
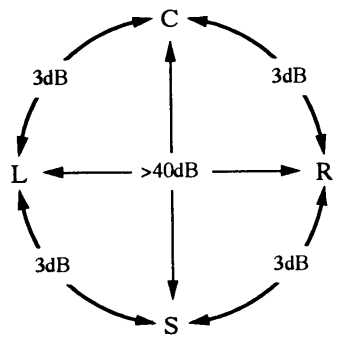


Fig. 4-6 Passive surround decoder separation map



1-7. Center Mode Control

1-7-1. ON/OFF Control

The easiest way to optimize the input signal balance is to mute the center channel output, adjust the balance control for minimum dialogue level, then turn the speaker back on. To make this possible, a center channel ON/OFF switch is used to mute the audio at the matrix decoder output, ahead of the bass splitting function (described in part C below).

1-7-2. Phantom/Normal Mode

Since the center channel speaker is a new element to home audio/video systems, one might not be readily available when first installing a Prologic surround decoder. The "phantom" mode prevents loss of the center channel information by splitting it equally to the left and right speakers. The user should, however, be encouraged to complete the system and switch to the "normal" mode as soon as possible in order to benefit from the full spatial capabilities of the system.

1-8. Noise Sequencer

Balancing the sound levels in two-channel stereo is simple and direct, but when three or four channels are used, the task becomes more difficult. To enable the user to accurately set system balance, a steady test signal is played in one channel at a time and the levels are adjusted until they match each other. A mid-frequency noise signal is used so that it will sound similar from all speakers in the system regardless of size or location. (Noise is preferred over single tones to avoid the effects of standing waves.)

The noise is automatically switched through the four channels, L-C-R-S, lasting about two seconds in each. (It can also be switched to a three channel sequence, L-C-R, for use in products having the Dolby 3 stereo.) Designed to drive an active decoder, the noise signal is level and phase "encoded" per Table 4-1 so that identical levels will appear at each output of the decoder.

Table 4-1 Noise sequencer outputs

Encoded channel	Lt out	Rt out
Left	0 dB	OFF
Center	–3 dB	–3 dB (in-phase)
Right	OFF	0 dB
Surround	–3 dB	–3 dB (inverted phase)

1-9. Three Channel Mode (Dolby 3 Stereo)

This mode is a subset of the Prologic adaptive matrix described in Part 1-6. Specifically, the surround output is muted and directional enhancement for surround signals is disabled as shown in Fig. 4-7.

Products with active decoding capabilities may offer users the three channel mode for L-C-R reproduction. One purpose of this is to provide good system performance until surround speakers are in place, just as the phantom mode allows using the system in the absence of a center speaker. In either case, however, spatial characteristics are compromised, so completion of the system should be encouraged.

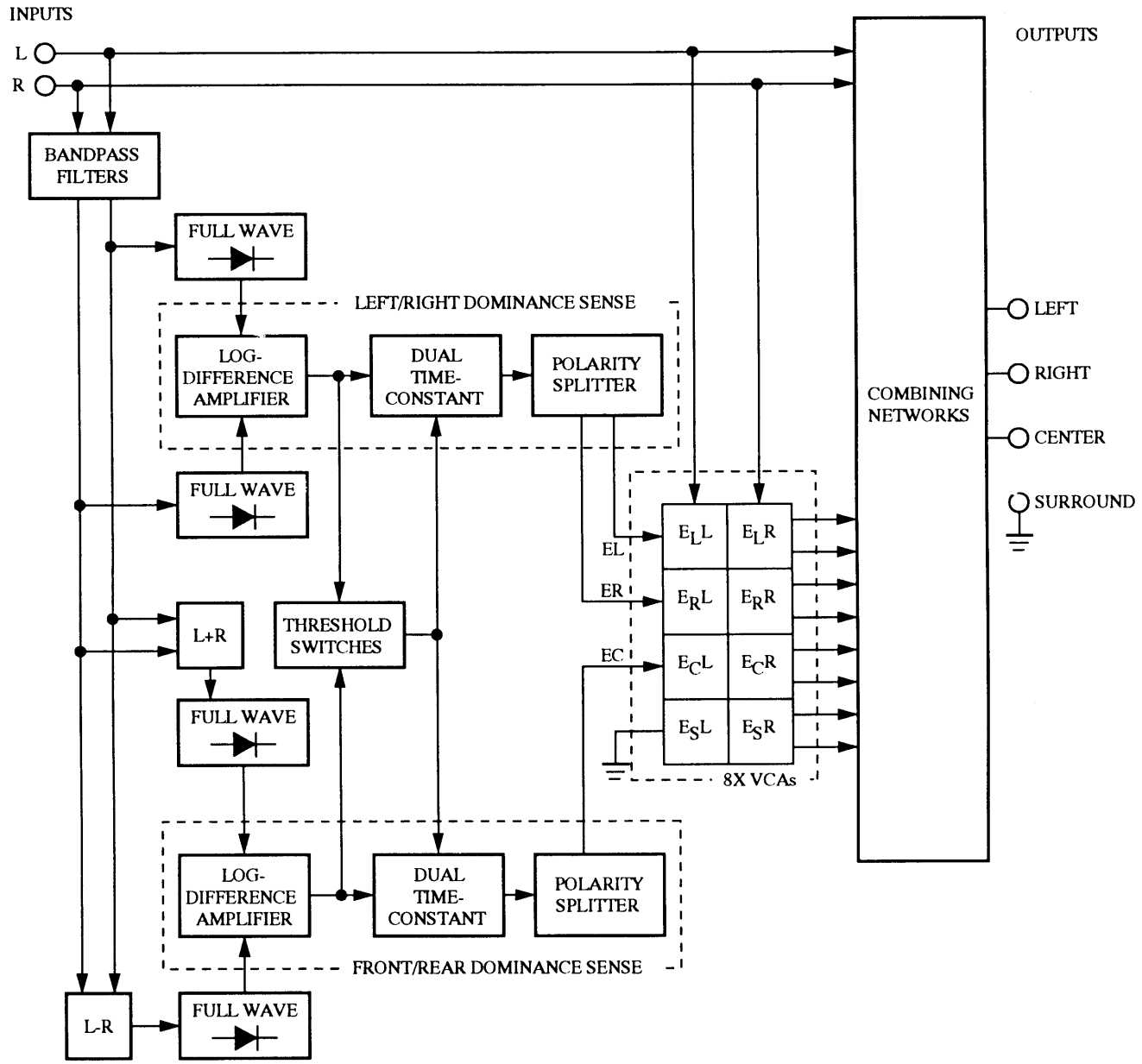
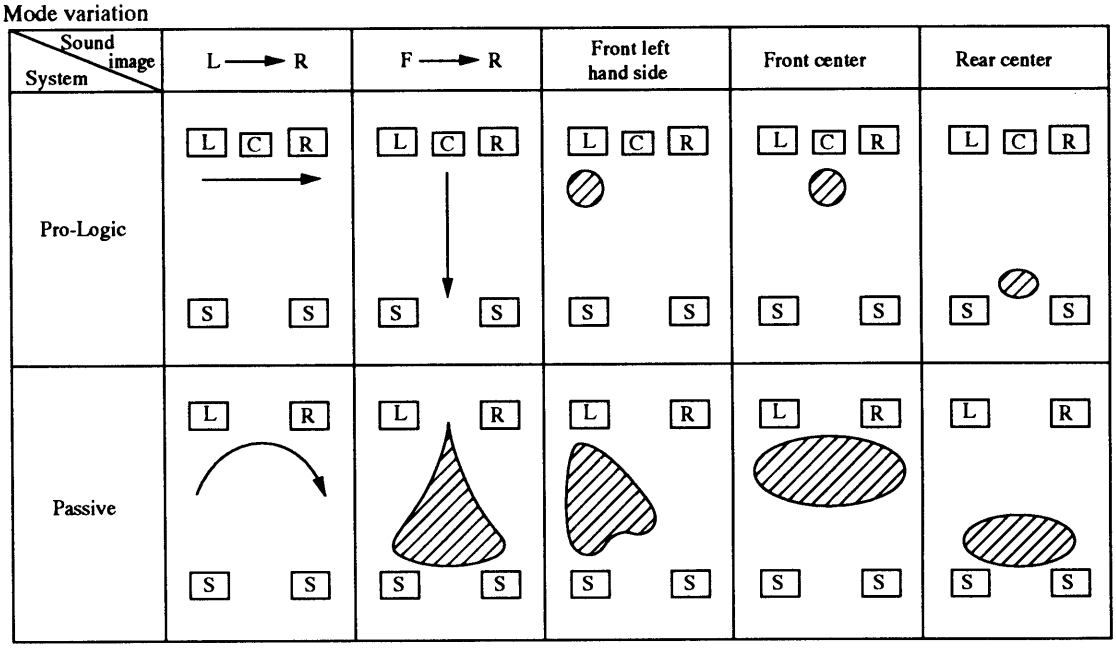
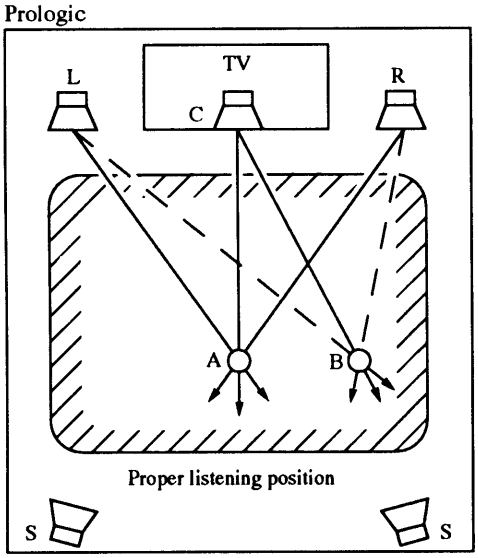


Fig. 4-7 Three channel adaptive matrix block diagram

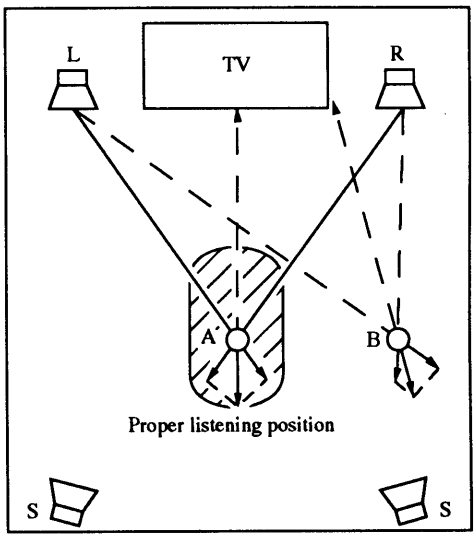
Mode variation



Prologic



Passive D-Surround



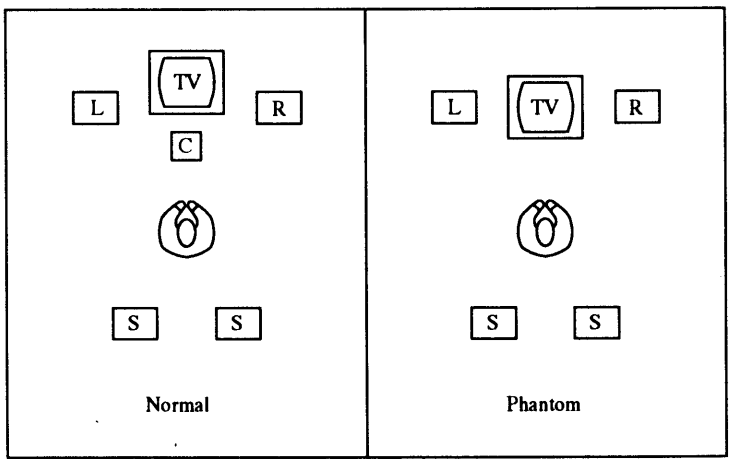


Fig. 4-8 Movement and Steering of Sound Image by Dolby Surround System Mode

1-10. Input Balance Control

This control allows the user to change program balance for optimum decoder performance. Since only mild levels of correction are needed, a control with as little as ±6 dB of range will be effective.

1-11. Anti-Alias Filter

The first block in the surround path is a filter to prevent spurious beat products occuring as a result of the sampling process in the time delay stage. Due to the wide range of sampling frequencies employed by a diversity of delay-line techniques (40 kHz for BBD to 2 MHz for Time Link ADM), the actual filter requirements will have to be tailored accordingly. As a further complication, noisy environments such as found inside television receivers can place additional demands on the filter to prevent picture-related radiation from interfering with the audio signals.

1-12. Audio Delay

Dolby Surround takes advantage of the "HAAS EFECT" or precedence effect to help reduce the perception of leakage signals from surround speakers. In order to do this, the decoder must compensate for the travel time of sound through air, which is approximately one foot per millisecond. By knowing the distance from the listening position to the front and surround speakers, a delay time of 20 ms is required.

1-13. 7 kHz Low-Pass Filter

Since the original surround signal was bandlimited to 7 kHz during encoding, this filter will improve processor tracking by preventing high-frequency audio signals from entering the decoder. The filter must have at least a 12 dB per octave slope above the breakpoint. In cases where strong delay line clock signals are present or where radiated high frequency signals from adjacent circuitry are picked up, the filter may need to be improved to prevent interference with the following noise reduction processor.

1-14. Modified Dolby B-type Noise Reduction

This final stage in the surround chain restores the signal to its original spectrum while reducing noise and certain crosstalk signals.

2. BLOCK DIAGRAM

2-1. Prologic Unit Block Diagram (PB4372)

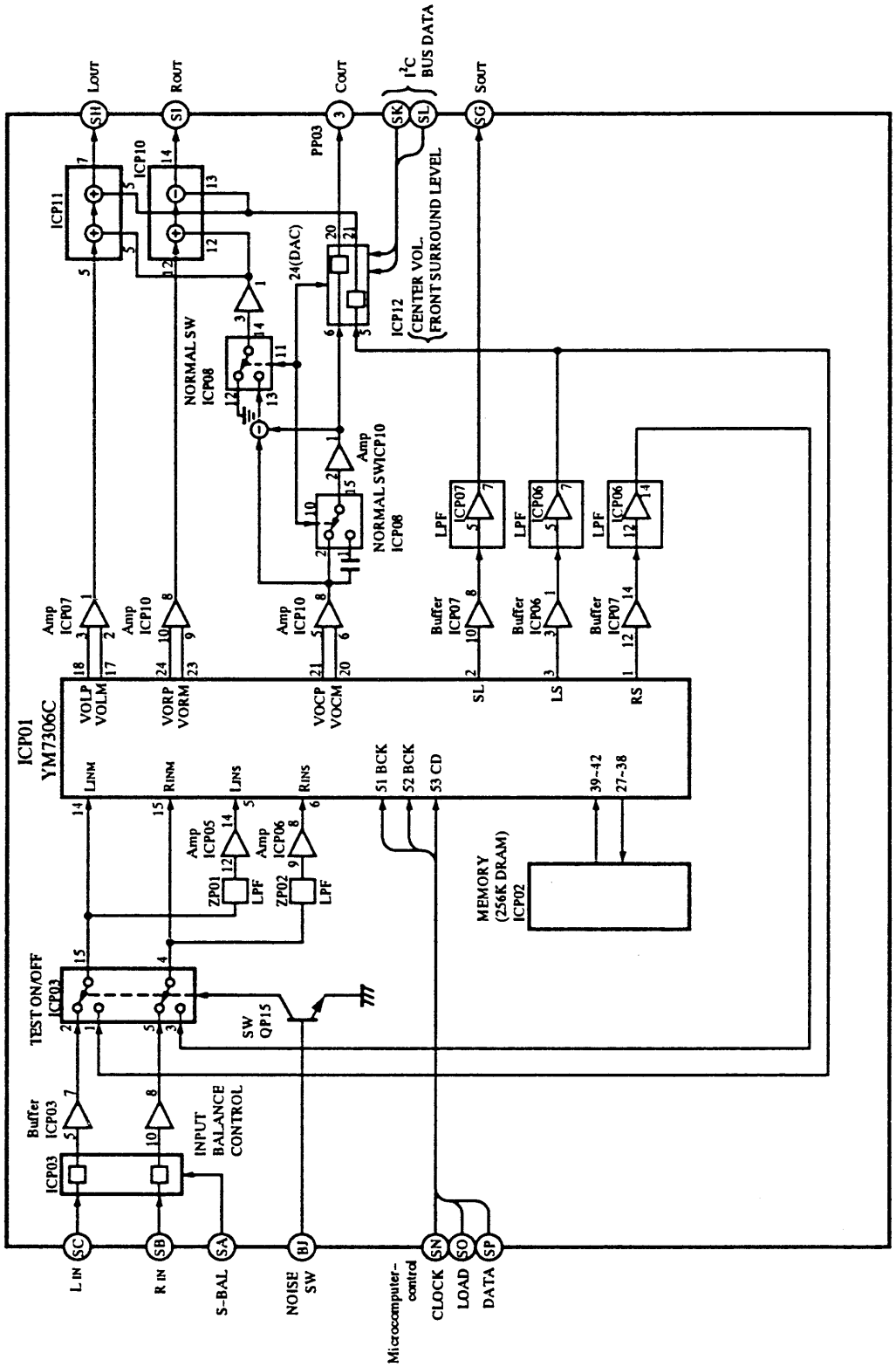


Fig. 4-9

2-3. Prologic Control Block Diagram of TW56D90

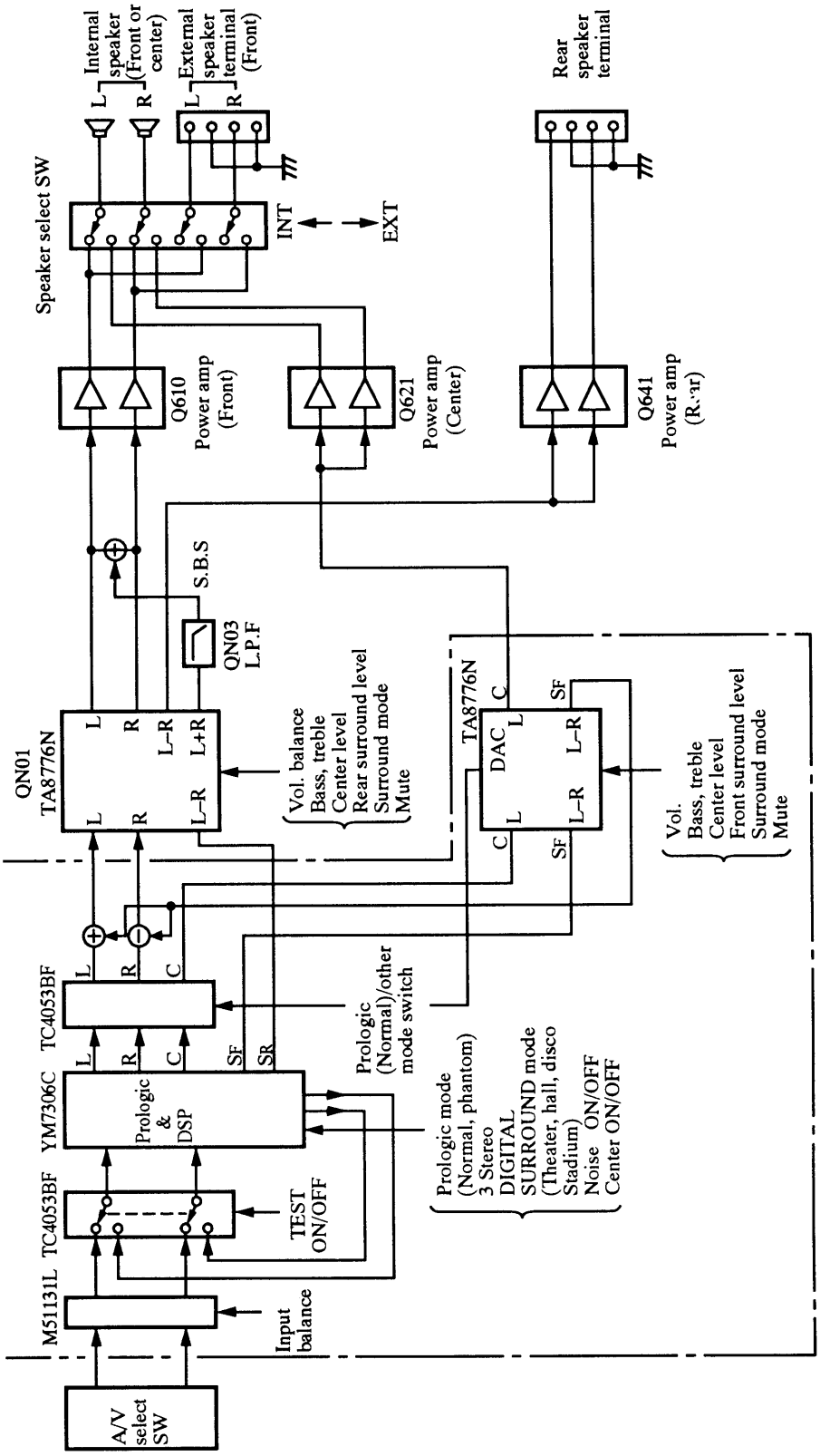
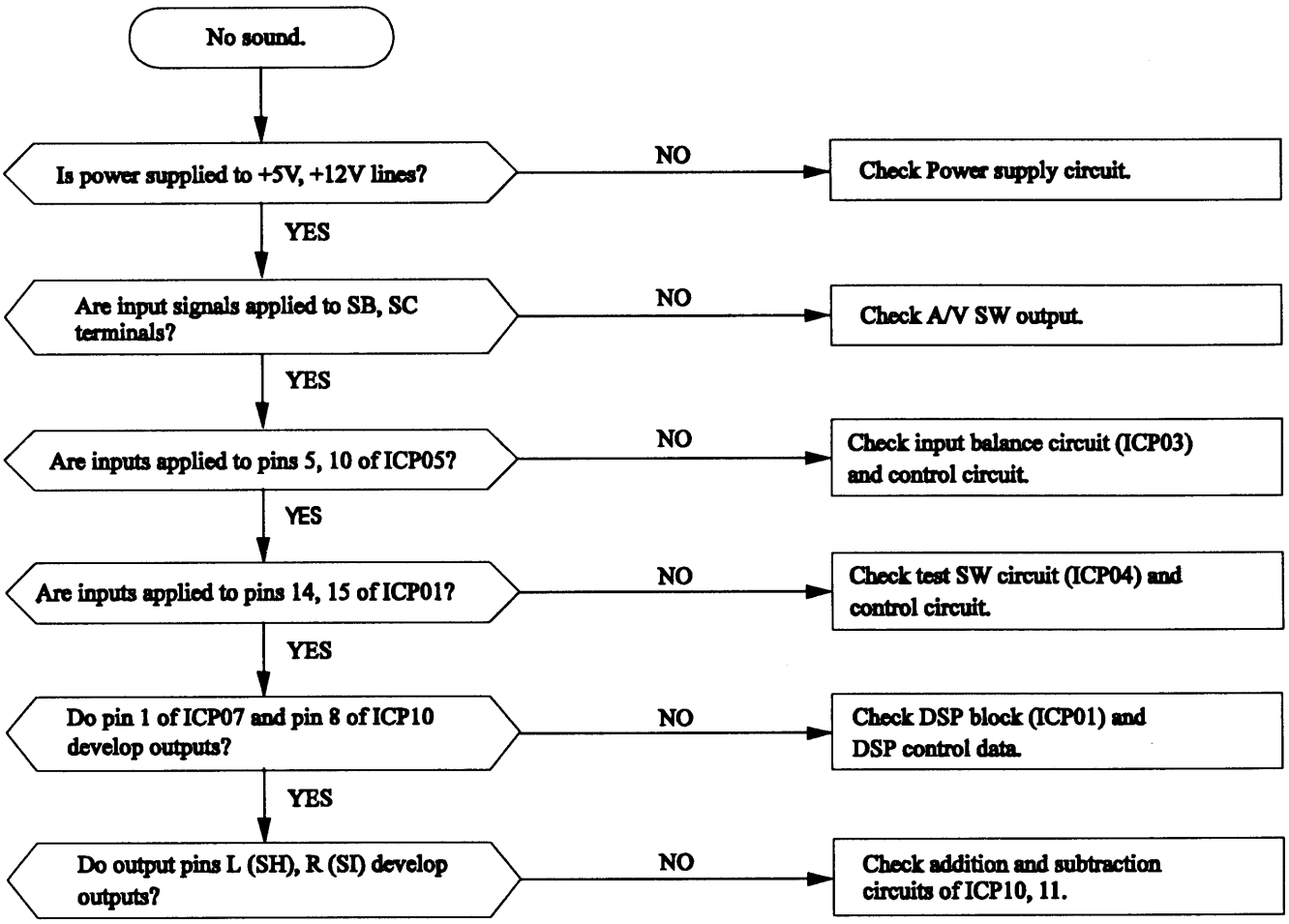
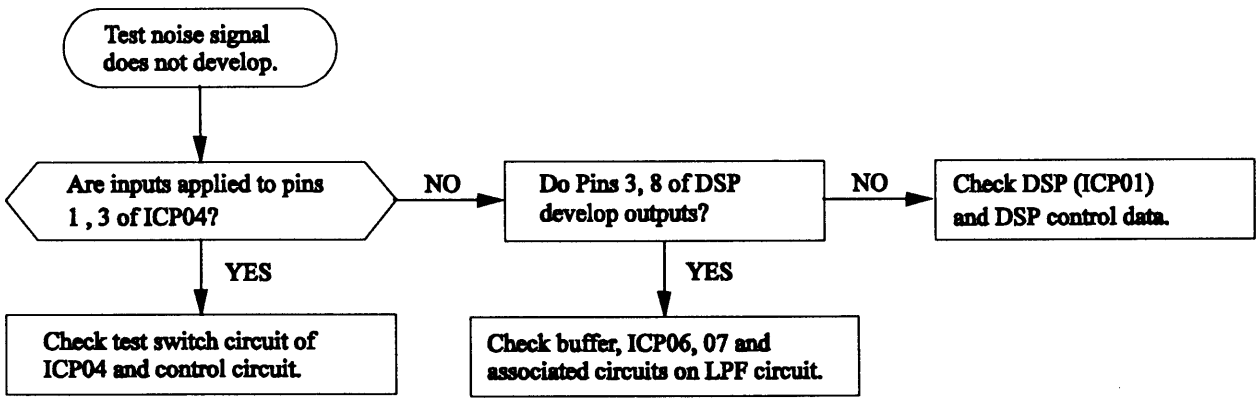
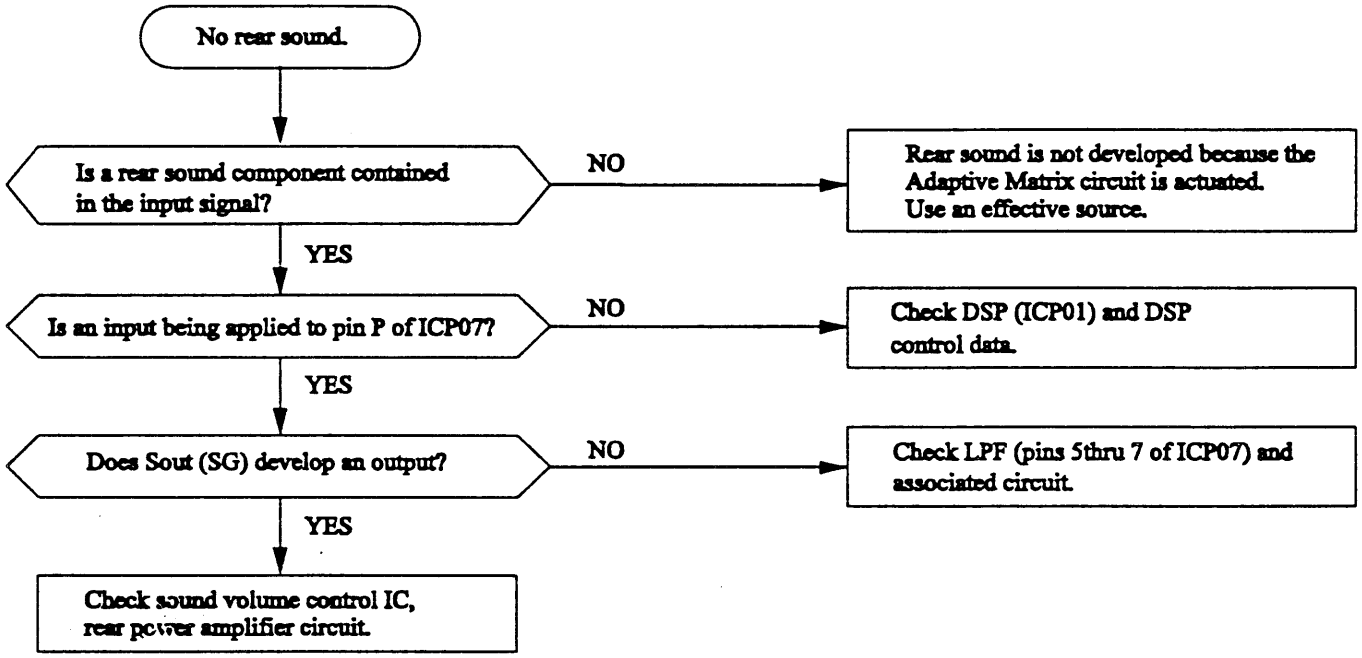


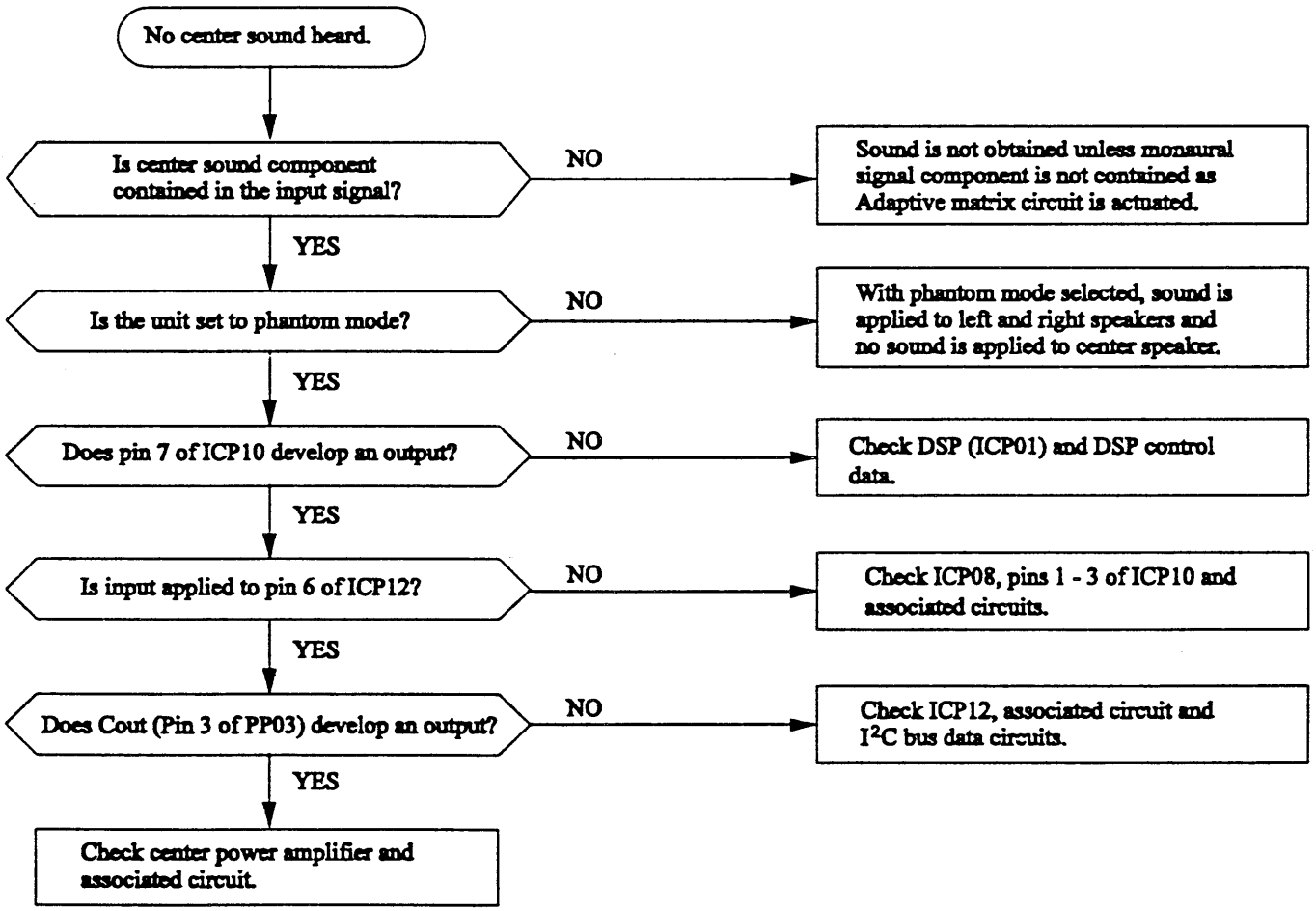
Fig. 4-11

3. TROUBLESHOOTING CHART






No rear sound.
Is a rear sound component contained in the input signal?
NO
Rear sound is not developed because the Adaptive Matrix circuit is actuated. Use an effective source.
YES
Is an input being applied to pin P of ICP07?
NO
Check DSP (ICP01) and DSP control data.
YES
Does Sout (SG) develop an output?
NO
Check LPF (pins 5thru 7 of ICP07) and associated circuit.
YES
Check sound volume control IC, rear power amplifier circuit.


No center sound heard.
Is center sound component contained in the input signal?
NO
Sound is not obtained unless monaural signal component is not contained as Adaptive matrix circuit is actuated.
YES
Is the unit set to phantom mode?
NO
With phantom mode selected, sound is applied to left and right speakers and no sound is applied to center speaker.
YES
Does pin 7 of ICP10 develop an output?
NO
Check DSP (ICP01) and DSP control data.
YES
Is input applied to pin 6 of ICP12?
NO
Check ICP08, pins 1 - 3 of ICP10 and associated circuits.
YES
Does Cout (Pin 3 of PP03) develop an output?
NO
Check ICP12, associated circuit and I2C bus data circuits.
YES
Check center power amplifier and associated circuit.

MEMO

SECTION V
CONVERGENCE CIRCUIT

1. INTERLACING IMPROVEMENT CIRCUIT IN WIDE SCREEN MODE

1-1. Block Diagram

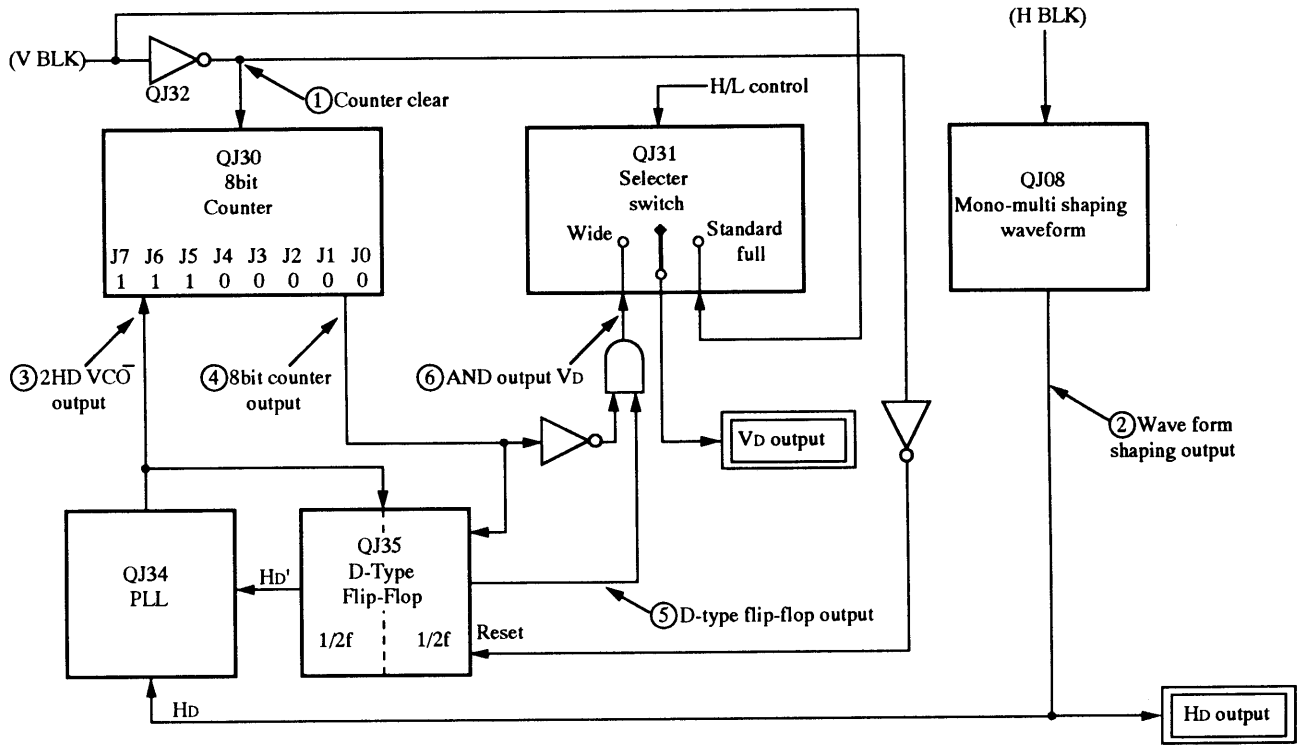


Fig. 5-1 Block diagram

In the WIDE screen mode, the video signal is shifted in advance by an amount of minus scroll under a data control and the picture moves upward to the raster screen (main deflection). To position the picture at center of the frame, a DC current is flown in the main deflection, thereby moving the screen downward and aligning the centers of the video signal picture and the frame of the set. In this case, a correction wave for the convergence is deviated in phase from that of the main deflection, so the circuit shown above is added. This circuit is to develop VD' which leads by Δ t in the phase of VD in the WIDE mode.

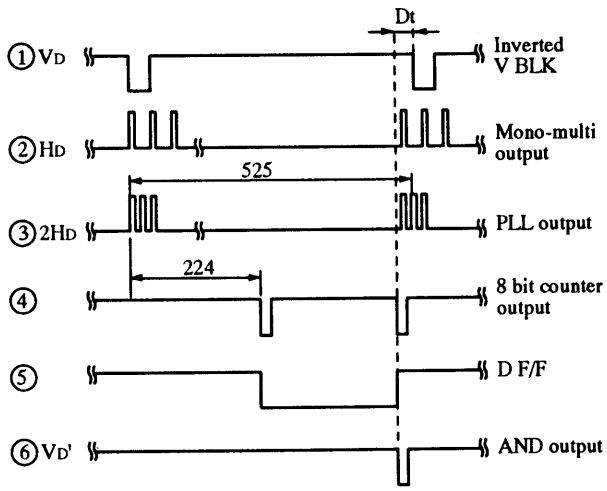


Fig. 5-2 Timing Diagram

1-2. Theory of Operation

1-2-1.VBLpart of VBLK entered from the main deflection circuit is inverted and clears the QJ30 8 bit counter (①). This output is further inverted and resets QJ35 D-type F/F.

The other part of VBLK enters one of two input terminals of QJ31 switch. An operation result of the D-type FF enters the other input terminals of the switch, thereby developing VD and VD' in the STANDARD/FULL and WIDE screen mode.

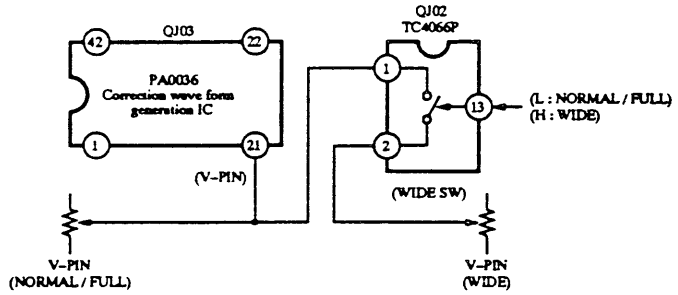
1-2-2. HBLK

In this circuit VD' output is created by making an operation with an HD obtained by wave shaping HBLK. The HD enters one of two inputs of QJ34 PLL phase comparator and a signal obtained by dividing the output into 1/2f in QJ35 enters the other input of QJ34. As a result, VCO output is developed at a timing of ③ 2HD from QJ34 PLL phase comparator. This output is counted by the 8 bit counter and the counted value reaches a setting value of 11100000, two values are developed for one V period. (Wave form ④). Thus obtained wave form signal is split into two: one is inverted and the other is counted down to 1/2f. Supplying both the outputs obtained in this way to the AND circuit develops the output ⑥. That is, VD' which is equivalent to VD advanced by Δ t is obtained.

Note:

If the HD is counted simply by the 8 bit counter, a different VD will be developed for an odd or even period. To prevent this, the counting operation is carried out with 2HD created in the PLL.

2. WIDE CONVERGENCE ADJUSTMENT



2-1. Block Diagram

2-2. Theory of Operation

In the NORMAL/FULL and WIDE modes, a convergence deviation occurs due to a difference in V amplitudes in each of the modes. Therefore, convergence adjustments are first accomplished in the NORMAL/FULL mode and then in the WIDE mode using additional controls.

2-3. Adjustment for NORMAL/WIDE

(1) Perform the adjustments by applying the waveform created by QJ03 (the convergence correction waveform IC) to NORMAL/FULL adjustment controls.

(2) In the WIDE mode, set the QJ02 switch to on and perform the adjustments while applying the signal to the WIDE adjustment control.

- WIDE switch controls the adjustment modes.
  L: NORMAL/FULL (SW = open),
  H: WIDE (SW = closed)

TW56D90 EEPROM and DIGITAL ADJUSTMENTS TABLE DATA

1. ADJUSTMENT OF VIDEO CORRECTION VALUE

Address	Items	Factory Setting STANDARD	After "Recall" STANDARD	FULL	THEATERWIDE 1, 2, 3
160H	Contrast	OE	0E	0E	0E
162H	Color in Theater	O7	O7	O7	O7
164H	Sharpness	OE	OE	OE	OE
165H	PIP-Contrast	OO	OO	OO	OO

2. SUB ADJUSTMENT

Address	Items	Factory Setting STANDARD	After "Recall" STANDARD	FULL	THEATERWIDE 1, 2, 3
107H	Sub-Color	92	90	90	90
108H	Sub-Contrast	FH	E7	E7	E7
105H	PIP-Bright	56	32	32	32
163H	Sub-Tint	49	52	52	52
161H	Sub-Bright	54	5D	5D	5D
111H	Monitor Switch	50	70	70	70

3. ADJUSTMENT OF Q501 (VCD)

Address	Items	Factory Setting STANDARD	After "Recall" STANDARD	FULL	THEATERWIDE 1, 2, 3
100H	Contrast	72	72	72	72
101H	Brightness	86	8F	8F	8F
102H	Color	4D	4D	4D	4D
103H	Tint	7B	84	84	84
104H	Sharpness	C0	C0	C0	C0
105H	PIP-Bright	56	32	32	32
106H	PIP-Contrast	E4	64	64	64
107H	SUB-Color	92	90	90	90
108H	SUB-Contrast	F4	E7	E7	E7
109H	R Cutoff	38	40	40	40
10AH	G Cutoff	40	40	40	40
10BH	B Cutoff	28	40	40	40
10CH	G Drive	40	40	40	40
10DH	B Drive	40	40	40	40
10EH	Chroma Control	A4	A4	A4	A4
10FH	Video Control 1	16	16	16	16
110H	Video Control 2	E1	E1	E1	E1
111H	HOR Position	50	70	70	70
112H	VER Position	23	23	23	23

NOTE: ALL DATA VALUES ARE IN HEXADECIMAL FORM. "H" DESIGNATION OMITTED FROM THE TABLES.

TW56D90 EEPROM and DIGITAL ADJUSTMENTS TABLE DATA

4. ADJUSTMENT OF OPTIONAL SWITCH

Address	Items	Factory Setting STANDARD	After "Recall" STANDARD	FULL	THEATERWIDE 1, 2, 3
174H	Option Setting	1O	1O	1O	1O
175H	Memory Version 1	OO	OO	OO	OO
176H	Number of Protect	OO	OO	OO	OO

5. DATA REVISION OF QA02 (E2PROM) *(Adjustment Screen is BLUE)*

Address	Items	Factory Setting STANDARD	After "Recall" STANDARD	FULL	THEATERWIDE 1, 2, 3
1D0H	STD Chroma Control	A4	A4	A4	A4
1D1H	STD Video Control 1	16	16	16	16
1D2H	STD Video Control 2	E1	E1	E1	E1
1D3H	Theater Chroma Control	6C	6C	6C	6C
1D4H	Theater Video Control 1	OO	OO	OO	OO
1D5H	Theater Video Control 2	37	37	37	37
1DAH	Option setting 2	OO	OO	OO	OO
1DBH	Option setting 3	OO	OO	OO	OO
1DDH	Memory version 2	OO	OO	OO	OO
1DEH	Theater R Cutoff Correct	OO	OO	OO	OO
1DFH	Theater G Cutoff Correct	OO	OO	OO	OO
1E0H	Theater B Cutoff Correct	OO	OO	OO	OO
1E1H	Theater G Drive Correct	F6	F6	F6	F6
1E2H	Theater B Drive Correct	F1	F1	F1	F1
184H		F8	F8	F8	F8
190H		OO	OO	OO	OO

6. ADJUSTMENT OF Q360 (Dynamic Pincushion Correction)

Address	Items	Factory Setting STANDARD	After "Recall" STANDARD	FULL	Theaterwide 1, 2, 3
120H	Vertical Height	39	3E	3E	61, 6D, 54
121H	Vertical Linearity	OC	OD	OD	O5, O5, O5
122H	Vertical S-Curve Correction	O7	O7	O7	O7
123H	Vertical Picture Correction	15	15	15	15
124H	Vertical Height Regulation	O8	O8	O8	O8
128H	Trapezoid Distortion	2O	2O	2O	2O
12AH	Vertical M-Curve Correction	OF	OF	OF	OF

NOTE: ALL DATA VALUES ARE IN HEXADECIMAL FORM. "H" DESIGNATION OMITTED FROM THE TABLES.

TW56D90 EEPROM and DIGITAL ADJUSTMENTS TABLE DATA

7. ADJUSTMENT OF QX60 (Wide Aspect)

Address	Items	Factory Setting STANDARD	After "Recall" STANDARD	THEATER WIDE 1, 2, 3	FULL
200H	Picture Size Change	62	62	62	62
201H	Picture Size Change	40	40	40	40
202H	Delay	F3	F3	F3	F3
203H	Delay	60	60	60	60
204H	B/A CL Width	72	72	72	72
205H	B/A CL Width	20	20	20	20
206H	Y Side Panel Level	EC	EC	EC	EC
207H	BLK Change Level	20	20	20	20
208H	IQ, QI Side Panel Level	OO	OO	OO	OO
209H	IQ, QI Side Panel Level	OO	OO	OO	OO
20AH	Y Signal Mem Write Clk	O7	O7	O7	O7
20BH	Start Position	OO	OO	OO	OO
20CH	C Signal Mem Write Clk	O6	O6	O6	O6
20DH	Start Position	C0	C0	C0	C0
20EH	Y,C Signal Mem W/R	73	73	73	73
20FH	Reset Position	OO	OO	OO	OO
210H	Y Signal Mem Read Clk	OF	OF	OF	OF
211H	Start Position	OO	OO	OO	OO
212H	C Signal Mem Read Clk	10	10	10	10
213H	Start Position	20	20	20	20
214H	Center Panel ► Side Panel	5F	5F	5F	5F
215H	Change Position	20	20	20	20
216H	Side Panel ► Center Panel	14	14	14	14
217H	Change Position	40	40	40	40
218H	Horizontal Blinking	72	72	72	72
219H	Start Position	OO	OO	OO	OO
21AH	Horizontal Blinking	O5	O5	O5	O5
21BH	Stop Position	OO	OO	OO	OO
21CH	Clamp Phase (Front)	7E	7E	7E	7E
21DH	Clamp Phase (Front)	OO	OO	OO	OO
21EH	Clamp Phase (Back)	7C	7C	7C	7C
21FH	Clamp Phase (Back)	OO	OO	OO	OO
220H	Hor. Drive Pulse Phase	OO	OO	OO	OO
221H	Hor. Drive Pulse Phase	OO	OO	OO	OO
222H	Horizontal Blinking	6F	6F	6F	6F
223H	Start Position	OO	OO	OO	OO
224H	Horizontal Blinking	O2	O2	O2	O2
225H	Stop Position	20	20	20	20
226H	Scan Velocity Modulation	60	60	80	80

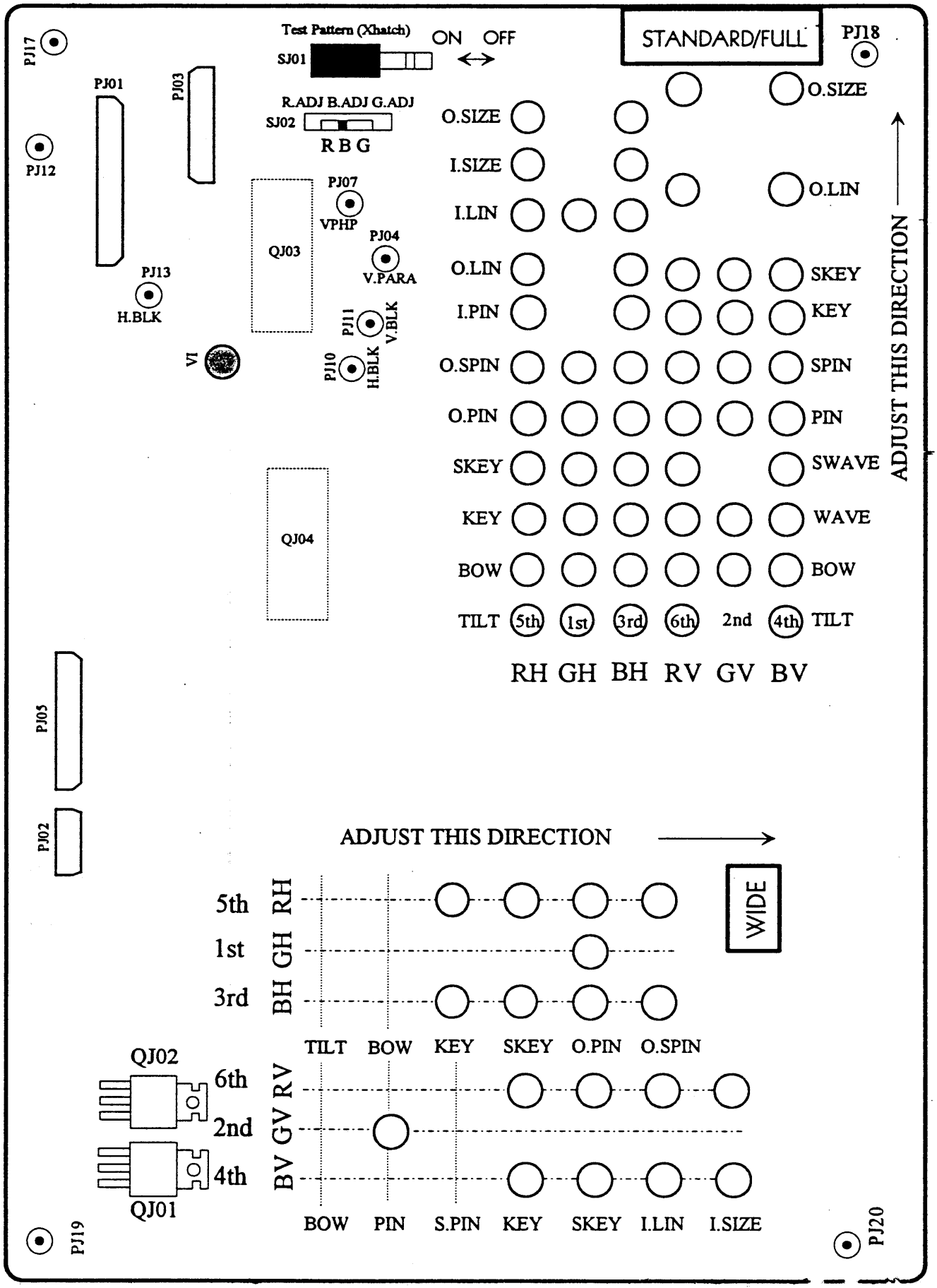
NOTE: ALL DATA VALUES ARE IN HEXADECIMAL FORM. "H" DESIGNATION OMITTED FROM THE TABLES.

TW56D90 EEPROM and DIGITAL ADJUSTMENTS TABLE DATA

201H	Picture Size Change	40	40	40	40
227H	Start Position	40	40	OO	OO
228H	Scan Velocity Modulation	15	15	OO	OO
229H	Stop Position	80	80	OO	OO
22AH	Input Signal Through	65	65	65	65
22BH	Start Position	OO	OO	OO	OO
22CH	Input Signal Through	O5	O5	O5	O5
22DH	Stop Position	E0	E0	E0	E0
22EH	Vertical Blinking	7F	7F	72, 6F, 76	7F
22FH	Start Position	20	20	E0, A0, 20	20
230H	Vertical Blinking	O8	O8	16, 19, 13	O8
231H	Stop Position	OO	OO	OO	OO
232H	V Drive Pulse Phase	OO	OO	09, 09, 0A	OO
233H	V Drive Pulse Phase	80	80	80, OO, 40	OO
234H	Vertical Signal Mask	O1	O1	O1	O1
235H	Start Position	OO	OO	OO	OO
236H	Vertical Signal Mask	O2	O2	O2	O2
237H	Stop Position	OO	OO	OO	OO
238H	IC Test Use Only	OO	OO	OO	OO
239H	IC Test Use Only	OO	OO	OO	OO
23AH	IC Test Use Only	OO	OO	OO	OO
23BH	IC Test Use Only	OO	OO	OO	OO
23CH	IC Test Use Only	OO	OO	OO	OO
23DH	IC Test Use Only	OO	OO	OO	OO
23EH	End Data	OO	OO	OO	OO
23FH	End Data	OO	OO	OO	OO

NOTES:

NOTE: ALL DATA VALUES ARE IN HEXADECIMAL FORM. "H" DESIGNATION OMITTED FROM THE TABLES.


Test Pattern (Xhatch)
ON OFF
SJ01
STANDARD/FULL
PJ17
PJ18
PJ01
PJ03
R.ADJ B.ADJ G.ADJ
SJ02
R B G
PJ12
PJ07
VPHP
PJ04
V.PARA
QJ03
PJ13
H.BLK
PJ11
V.BLK
VI
PJ10
H.BLK
QJ04
O.SIZE
I.SIZE
I.LIN
O.LIN
I.PIN
O.SPIN
O.PIN
SKEY
KEY
BOW
TILT
5th
1st
3rd
6th
2nd
4th
SKEY
KEY
SPIN
PIN
SWAVE
WAVE
BOW
TILT
ADJUST THIS DIRECTION
RH GH BH RV GV BV
PJ05
PJ02
ADJUST THIS DIRECTION
WIDE
5th RH
1st GH
3rd BH
TILT BOW KEY SKEY O.PIN O.SPIN
QJ02
6th
2nd
4th
BV GV RV
QJ01
BOW PIN S.PIN KEY SKEY I.LIN I.SIZE
PJ19
PJ20

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